

Lithographic Chip Identification: Meeting the Failure Analysis Challenge

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Abstract

This paper describes a novel method using stepper photolithography to uniquely identify individual chips for permanent traceability. A commercially available 1X stepper is used to mark chips with an identifier or “serial number” which can be encoded with relevant information for the integrated circuit manufacturer.

The permanent identification of individual chips can improve current methods of quality control, failure analysis, and inventory control. The need for this technology is escalating as manufacturers seek to provide six sigma quality control for their products and trace fabrication problems to their source. This need is especially acute for parts that fail after packaging and are returned to the manufacturer for analysis. Using this novel approach, failure analysis data can be tied back to a particular batch, wafer, or even a position within a wafer. Process control can be enhanced by identifying the root cause of chip failures.

Chip identification also addresses manufacturers concerns with increasing incidences of chip theft. Since chips currently carry no identification other than the manufacturer’s name and part number, recovery efforts are hampered by the inability to determine the sales history of a specific packaged chip. A definitive identifier or serial number for each chip would address this concern.

The results of chip identification (patent pending) are easily viewed through a low power microscope. Batch number, wafer number, exposure step, and chip location within the exposure step can be recorded, as can dates and other items of interest. An explanation of the chip identification procedure and processing requirements will be described. Experimental testing and results will be presented, and potential applications discussed.

1. Introduction

As quality and process control requirements escalate with six sigma requirements, it is vital that the chip manufacturer determine and eliminate the causes for chip failure. A method has been developed, using an Ultratech 2000 Series stepper, to uniquely identify any and all chips with a “serial number” for permanent traceability. This method, called chip identification, employs the Ultratech 2000 Series of steppers and a simple lithography procedure to place a unique identifier on each chip.

Historically, methods of identifying chips included placing row and column numbers on contact print masks. This capability was lost as the industry moved toward stepper technology where the image is repeated multiple times on a wafer. Although the contact print method provided a permanent indication of chip location on a wafer, the wafer number and batch identification were not available after chip packaging.

With the Ultratech chip ID method, information such as batch number, wafer number, exposure step, chip location within the exposure step, and date can be recorded for complete chip identification. Manufacturers seeking the cause of a failure of a packaged chip can determine the complete processing history of the chip from the chip ID and their own documentation of the chip's processing.

Chip identification can also effectively address manufacturers concerns with increasing incidences of chip theft. In 1989 the insurance industry estimate of chips stolen in California alone was \$20 million¹. Since chips currently carry no identification other than the manufacturers name and revision numbers, recovery efforts are hampered by the inability to determine the sales history of a specific packaged chip. A definitive identifier for each chip, in conjunction with a computerized data base, would address this concern.

The chip identification method (patent pending) was developed at Ultratech and tested at the TRW Microelectronics Center. It is simple for a chip manufacturer to implement and use, and the results are easily viewed through a microscope at low power.

2. Description of the Ultratech Alignment System

2.1 Projection Lens

In order to understand chip ID methodology, a general understanding of the principles of the Ultratech is needed. The Ultratech Stepper utilizes the Wynne-Dyson-Hershel 1X lens. This nearly concentric and symmetrical design is free from Seidel aberrations. The lens is mounted on the stepper with its optical axis at 17° to the travel of the stepper's linear motor XY wafer stage. The input and output prisms provide for the separation of the reticle (object) and wafer (image) planes. The reticle resides on a precision air slider attached to the reticle stage which itself is mounted to the lens housing. Due to the proximity of the reticle stage to the wafer plane, the precision XY wafer stage can be used to load and accurately position reticles on the reticle stage.

2.2 Alignment System

Precision reticle loading and wafer alignment is accomplished through the use of Ultratech's unique through-the-lens alignment system. The theory and practical description of the alignment system has been previously well documented². For the purpose of this paper it is necessary to know that the alignment system incorporates a small hole at the center of the primary mirror along with collection optics, a crossmask (field stop) and detector, all of which are mounted behind the primary mirror and exterior to the lens housing (Figure 1). The crossmask is a conjugate plane of both the reticle and wafer. Crossmask positioning is determined at initial machine setup and thereafter becomes the reference for reticle loads and wafer aligns.

2.3 Reticle Loading

During reticle loads, fiducials on the reticle are scanned across and aligned to the crossmasks using the stepper's alignment system. Precise positioning of the reticle in the X axis is achieved by the linear motor XY wafer stage. Precise positioning of the reticle in the Y axis is also made by the linear motor XY wafer stage which is used to adjust ramp mechanisms on the reticle slider. The lateral motion of the XY wafer stage engaged in the Y ramps drives the reticle in the Y axis to the position learned during fiducial scanning. Typical reticle positioning precision is **2.5 µm** 3 sigma in X and **1.2 µm** 3 sigma in Y.

2.4 Multiple Field Reticles

Reticles are in either of two formats, 3x5" quartz plate with guides attached on the glass side at the two lower comers, or as an uncut 5x5" quartz plate. A feature of

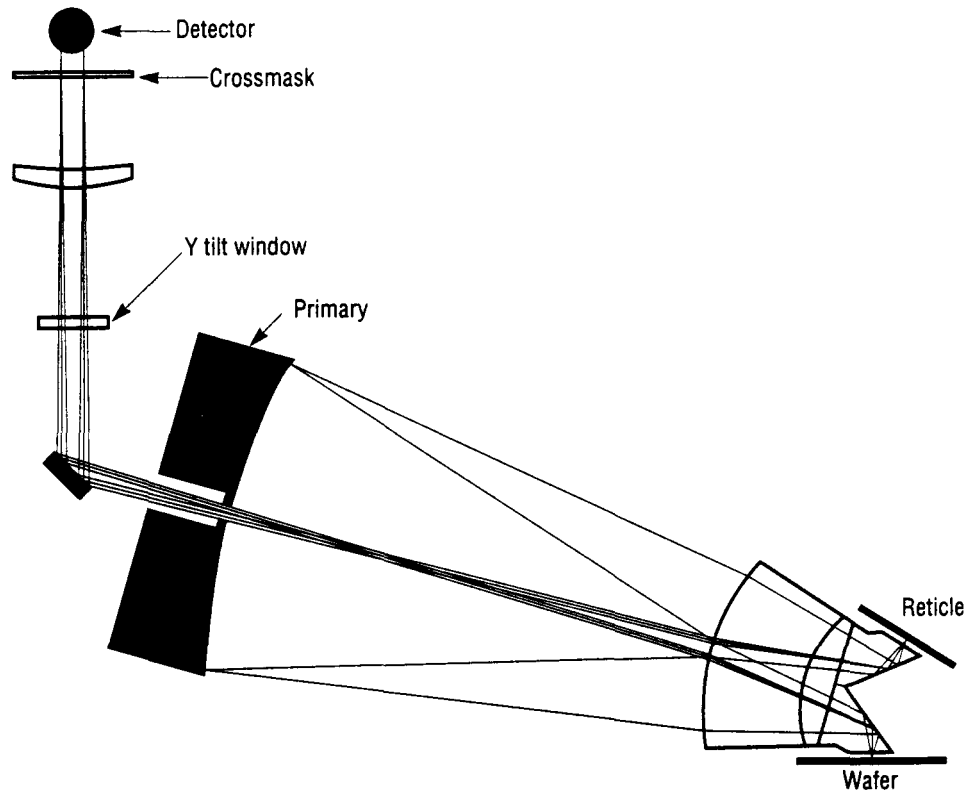


Figure 1. Ultratech Stepper Alignment System

the 1X lens, by virtue of the fact that object and image size are equal, is that as many as seven fields can be contained on a single reticle. Using the widest specified field size of 39.0mm x 11.4mm, two fields per reticle can still be accommodated. Depending on the circuit design, each reticle field may contain multiple die. The algorithm for reticle loading includes measuring and adjusting reticle skew and recording any remaining offsets. Reticle skew error translates to intrafield theta error and, with multiple field reticles, interfield Y translation error at the wafer plane. These offsets are accounted for by Enhanced Global Alignment (EGA) during wafer alignment and in the case of drop-in fields when reticle field changes are required. Also, in the case of multiple field reticles, field pitch error is determined, which is the result of reticle error and/or tilt in the X axis of the reticle plane. Similarly, any offset is accounted for when changing between fields of a multiple field reticle.

The automated alignment of reticles and the programmable option to choose among multiple fields per reticle with quick, seven second field changes, provides the flexibility to expose multiple fields per wafer. This ability lends itself to the insertion of test fields, the placement of uniquely different chips on the same wafer, the utilization of voting lithography, as well as to the techniques of the Ultratech chip identification method,

3. Design Requirements

Before starting the development project it was necessary to define the required output of a chip identification method:

- The method must be simple to use and virtually invisible to the operator.
- The identification mark (ID) must be easily viewed through a microscope.
- The ID must be in plain text format, without requiring interpretation or data translation.
- The ID must be able to provide a variety of information that is relevant to the manufacturer. The minimum identifying information would be batch number, wafer number, and chip location number on the wafer. Additional information such as date, operator ID, or processing information must be easily incorporated as required.
- The ID area must be small, preferably no larger than $200 \times 200 \mu\text{m}$, since it must be located within the die itself.
- The location of the ID area in the die must be flexible since the available space will vary with product type.
- The ID must be easy to place in the chip design, with a minimum amount of effort on the part of the design or layout team.
- The ID procedure must not significantly effect overall stepper throughput or cost-per-wafer processed.

4. Design Concept

Based on the design requirements, the design concept can be described as follows:

- There is an area within each die dedicated to chip ID and identified as the ID grid.
- The ID grid contains an array of numbers and / or alphabetic characters corresponding to the amount and type of identifying information required. A sample layout of an ID grid is shown in Figure 2. The ID grid is placed within an existing process level which supplies good process contrast for resolution and ease of readability.
- Each ID grid is appropriately labeled denoting ‘wafer’, ‘step’, for each type of information.
- In cases of lithographic fields containing multiple chips, the chip number within the exposure field is directly inscribed near the grid. The chip number indicator is added at the time of field construction of the reticle.
- The number or alphabetic character corresponding to the correct identification information is exposed or “punched” during the chip ID procedure. This occurs at an existing process level subsequent to the grid placement.

W	1	6	11	16	21	26	31	36	41	46
A	2	7	12	17	22	27	32	37	42	47
F	3	8	13	18	23	28	33	38	43	48
E	4	9	14	19	24	29	34	39	44	49
R	5	10	15	20	25	30	35	40	45	50
S	1	6	11	16	21	26	31	36	41	46
T	2	7	12	17	22	27	32	37	42	47
E	3	8	13	18	23	28	33	38	43	48
P	4	9	14	19	24	29	34	39	44	49
P	5	10	15	20	25	30	35	40	45	50
B	A	B	C	D	E	F	G	H	I	J
A	K	L	M	N	O	P	Q	R	S	T
T	U	V	W	X	Y	Z				
C	1	2	3	4	5	6	7	8	9	0
H	1	2	3	4	5	6	7	8	9	0

C H I P 3

Figure 2 ID Grid

In Figure 2, the batch number **Z39**, wafer number 8, exposure step number **43**, and chip number 8 are identified through the chip ID procedure

5. Procedure

In order to implement chip ID, two image fields, usually on two different reticles must be modified. For the first layer, hereafter referred to as “layer A”, an ID grid is designed into the circuit area. This has no impact on reticle cost for this layer. This process layer should have good image contrast when viewed through a low power microscope and a minimum resolution of **2µm** to effectively image the grid numbers and dividing lines. In addition, it must be an etched layer, with the resulting patterns clearly visible after all wafer processing is complete.

During wafer processing, the ID grid is imaged concurrently with the circuit die during the standard exposure sequence for the process layer A. The pattern is etched and the wafers continue through the standard processing sequence for the given technology.

The second reticle modified, “layer B”, is typically a non-critical layer in the process, such as passivation. One field of the Ultratech multiple field reticle is dedicated as the ‘punch field’ and performs the marking of the ID grid. This allows for quick and convenient utilization of the punch field and ID marking procedure while performing standard wafer alignment and exposure. Because Ultratech reticles contain multiple fields, the use of the punch field has a minimal effect on total reticle cost. The graphic in Figure 3 represents the exposure of the chip ID grid at layer A. Figure 4 represents the punch exposures at layer B. In this example the image field contains four die, each die has an ID grid, and the reticle punch field has four corresponding indicator punches. When Layer A and B are correctly aligned, each punch resides in the upper left hand corner of its corresponding ID grid.

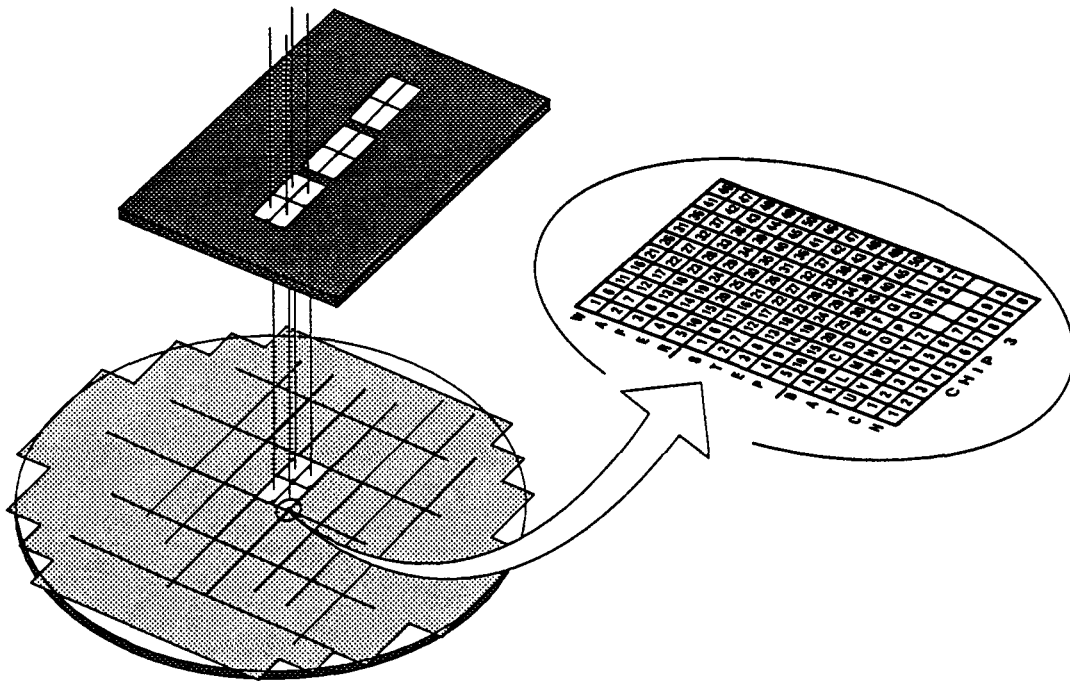


Figure 3. Exposure of Chip ID Grid (Layer A)

The chip identification punching procedure is performed at layer B in conjunction with the exposure of passivation level or a similar process layer. The operator selects the chip identification run mode. Typical operator input at this time might include batch number and/or wafer sequence (if the wafers are not processed in numerical order). With the passivation reticle image field, the wafer is automatically aligned and exposed in enhanced global alignment (EGA) mode. While the wafer remains on the wafer stage, the punch field is automatically repositioned for imaging. It is not critically aligned to the crossmasks since no

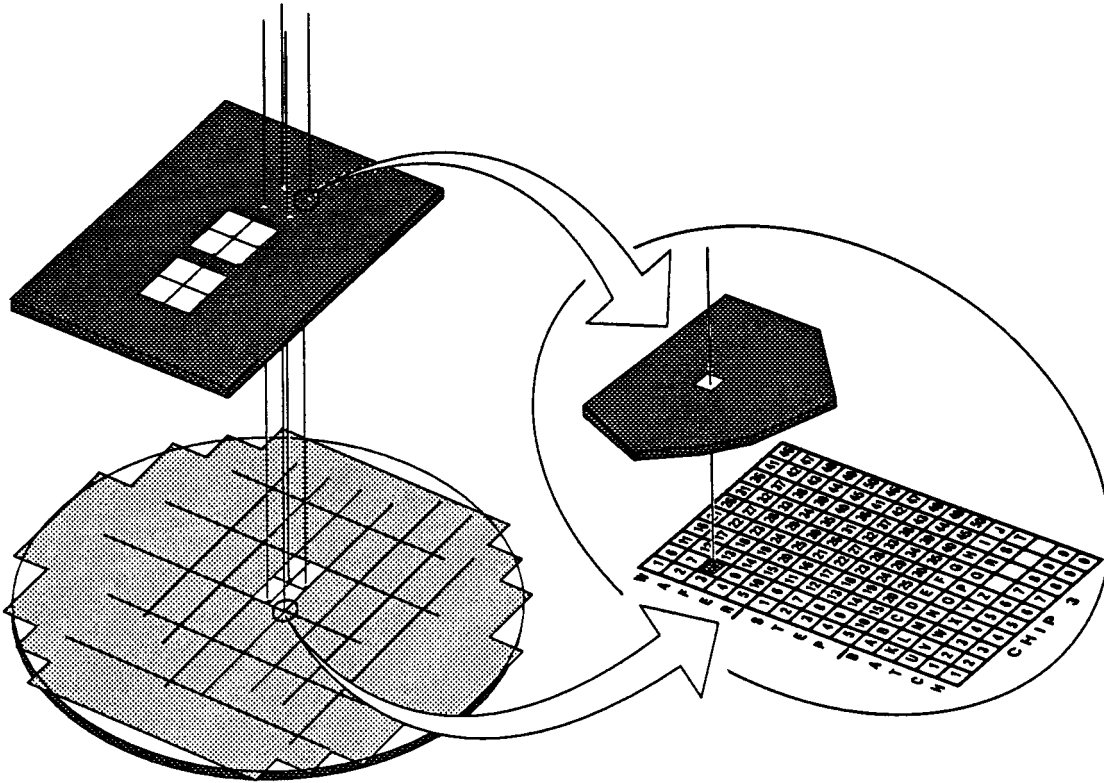


Figure 4. Exposure of Punch Field (Layer B)

keys are contained in the punch field. The wafer is mechanically aligned to expose the punches onto the correct numbers/letters on the grid. The number of punch exposures at each image step is determined by the amount of identifying information required. Because the chip number within the image field is defined in conjunction with the imaging of the ID grid at layer A, this saves an exposure step at layer B. After wafer load and unload, the reticle is repositioned at the product field and the cycle repeats for all successive wafers.

If the process contrast and design rules allow, layer A and B could be combined so that the chip ID grid imaging and punching are performed during the same process step.

6. Experimental

Experimental testing was segmented into in-house testing and an evaluation at a customer site. For in-house testing, a test reticle set was manufactured with wafer number, exposure number, and step number identifiers. It was used to troubleshoot the chip ID methodology including software and hardware. Because throughput of the chip ID procedure was an important consideration, stage settling and focus tolerances were relaxed to allow it to run faster at process layer B. The resulting punch accuracy and resolution were measured and the tolerances optimized through an iterative process. The reticle set contained a variety of grid sizes in order to determine the minimum working size.

When the chip ID procedure had been optimized in-house, TRW incorporated it into a product reticle set for production viability testing. TRW manufactures high speed bipolar class S parts for space applications. The reliability requirements for these parts are extensive as are the burn-in and failure analysis requirements. Chip ID is particularly relevant for these applications.

7. Results

7.1 Grid/Punch Size

The small sequentially numbered boxes within the chip ID grid are defined as “cells”. For a cell to be correctly marked with the punch, the majority of the punch must be in the cell. The correct grid cell must always be punched for acceptance.

In the in-house test reticle set, three sizes of cells (20x10, 15x10, and 10x10 microns) were tested to determine the minimum cell size. Cell size is defined as center-to-center distance; the dividing lines are two microns wide. In all cases, the punch size was 6x4 microns. In-house testing was performed on a Ultratech model 1500 stepper. It was determined that the punch accuracy was largely a function of the mechanical alignment and reticle positioning accuracy of the stepper. The reticle skew tolerances were tightened to ± 0.05 mrad for the loading of the reticle containing the punch field. With the relaxed stage and focus tolerances, and the resulting blindstep, the minimum cell size was determined to be 15x10 μm . Figure 5 is a photograph of the 15x10 micron cell size of the in-house test reticle set. In this case, the identification is wafer number one, field (exposure step) number eighteen, and chip number eleven within the exposure step. The total chip ID grid size is 165x150 μm .

For the TRW application, relatively few batches of each type of class S chips are run each year. The simplest method of identifying batch number was with a

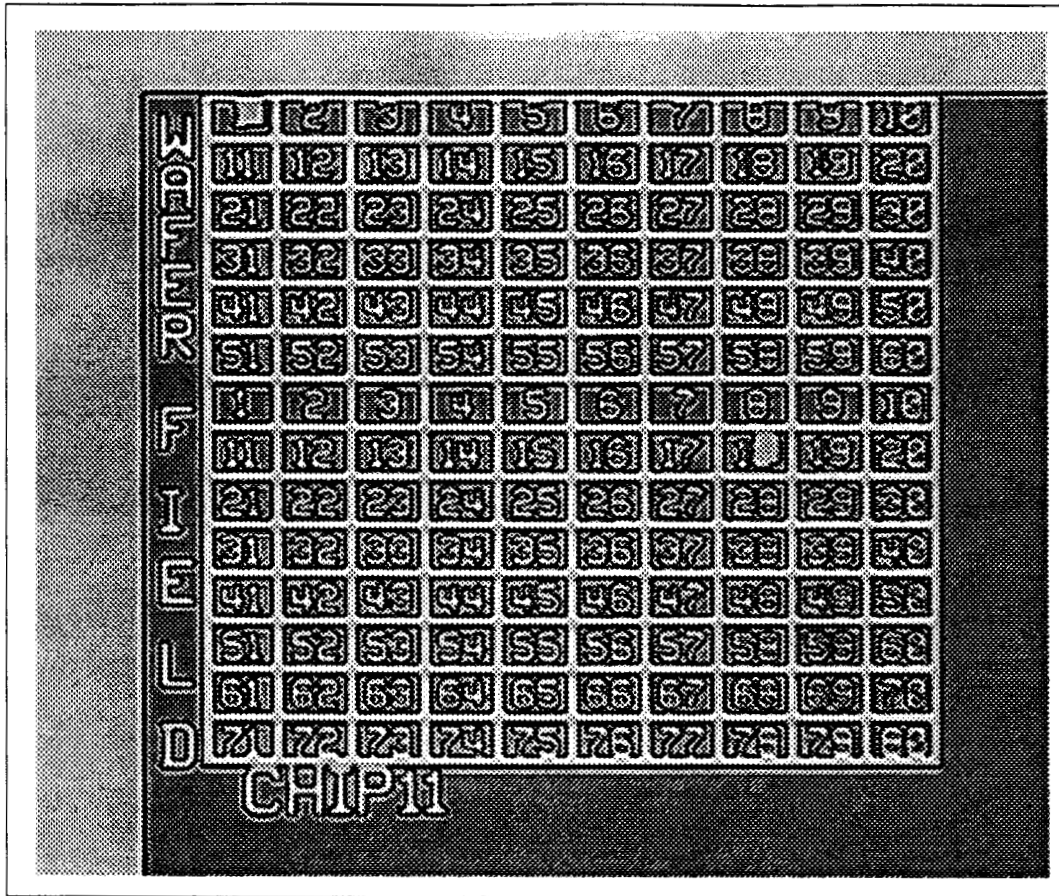


Figure 5. Ultratech Chip ID Grid

number sequence and the year. This is shown in Figure 6 with a photograph of a chip ID grid from a production reticle set. Batch number thirteen of year 1992, wafer number one, step number ten and left chip (of a two chip field), are identified with a 15x10 micron cell size. The ID grid was imaged at the second metal layer and punched at passivation. The punch size is 6x4 μm and the overall chip ID grid size is 165 x 210 μm .

The 2000 Series features a precision, monolithic, linear motor stage. Due to this superior stage design, the mechanical alignment capability of the 2000 Series is significantly better than that of the model 1500 (.07 μm versus 1.5 μm) The reticle loading routines have also been improved for more precise reticle positioning. It is expected that the minimum grid size on the 2000 Series should be smaller than that of the model 1500. Preliminary results have confirmed this assumption.

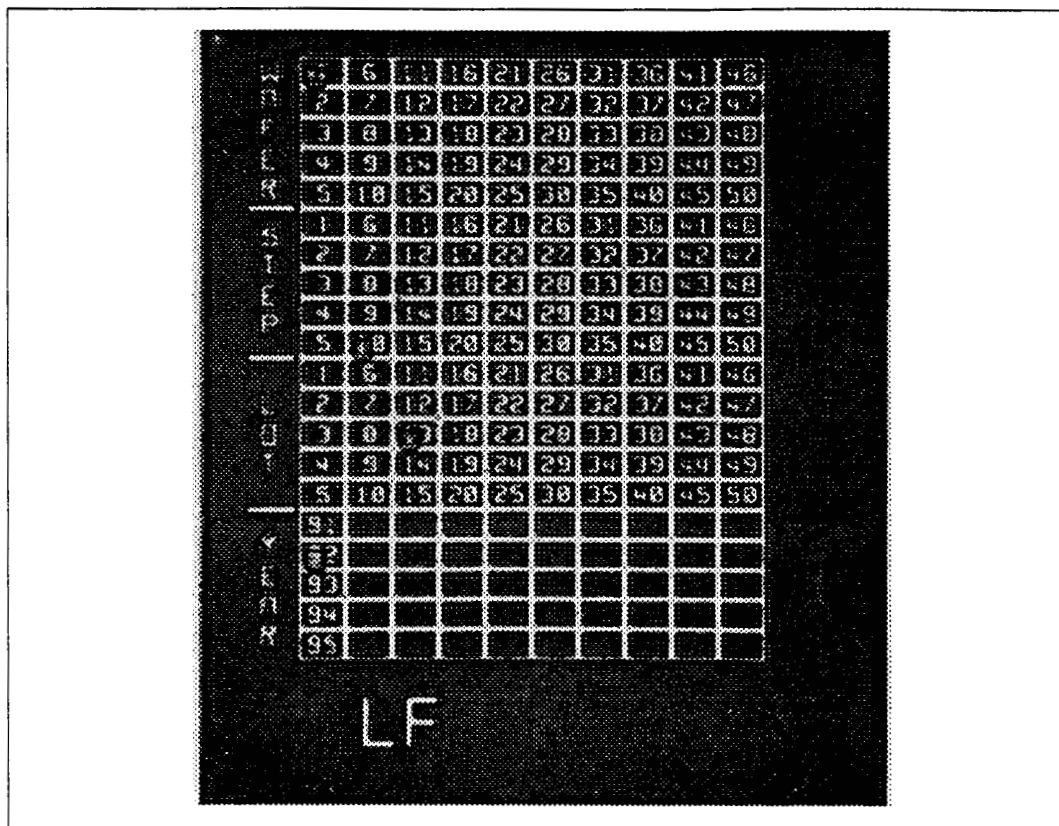


Figure 6. TRW Chip ID Grid

7.2 Resolution/Overlay

The resolution and overlay of layer B (passivation) was determined for the relaxed focus and stage settling tolerances. For the in-house test reticle set, resolution features started at one micron and increased in one micron increments. The two micron features resolved in all the tests and the one micron features usually resolved. Overlay results were better than $\pm 0.4\mu\text{m}$ total range. Because the punch was performed at passivation layer for TRW, overlay and resolution features were not available.

Since the focus and stage tolerances used for chip ID punching are only relaxed at a non-critical level such as passivation, the resulting overlay and resolution exceeds standard design rules.

7.3 Throughput

Throughput is largely dependent on the number of punch exposures required by the manufacturer for identifying information. The chip number within the exposure step is defined at layer A, so a punch step for chip number is not required at layer B. For comparison purposes, all throughput calculations were made using

100 ms exposures. The specified throughput for the M2020i stepper is **74** wafers per hour at **39** exposure steps.

Figure 7 is a graph of throughput for 6" wafers as a function of the number of identification punches and exposure steps on an M2020i stepper. It should be noted that this throughput table applies to layer B (passivation) only and includes both the alignment and exposure of process layer B, and the chip identification punch steps. Since chip identification does not effect throughput for any other process layer, the average throughput decrease for a 15 layer process with four chip ID punches would be 4%.

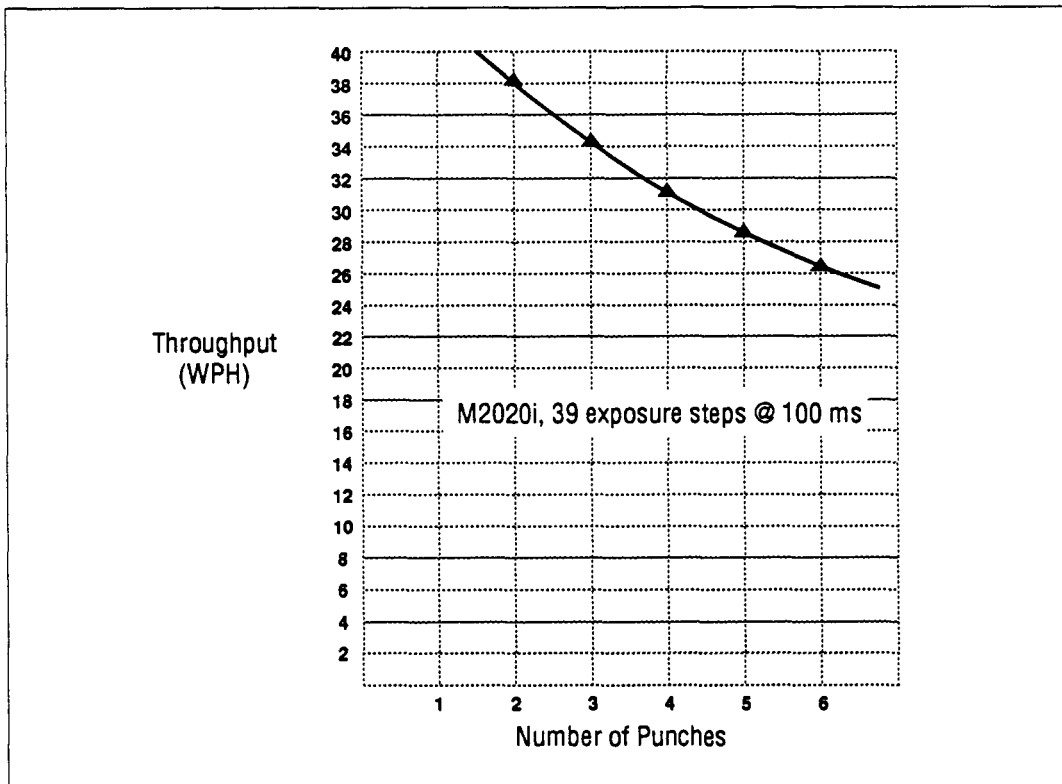


Figure 7. Throughput Versus Number of Punches

7.4 Design Issues

At the TRW test site, it was noted that the quickest implementation technique was to notify the designers ahead of floor planning for the die to allow space for the chip identification grid. In this way, the grid structure is simply dropped in during field construction and border attach. The ID grid could be placed at any convenient location within the die. Frequently it is possible to drop in the chip ID grip near the bonding pads even if no space was allocated during floor planning.

7.5 Reticles

The impact to reticle production at TRW was minimal. Chip identification required one extra field on the passivation reticle. The added cost to reticle production was estimated at 1% of total reticle cost.

7.6 Modifications

The examples of chip ID grids shown were for specific applications at Ultratech and TRW. Through factory software changes, grid size, layout, and type of identifying information can be modified to accommodate each manufacturer's needs.

8. Conclusions

A process for uniquely identifying individual chips with a “serial number” has been developed and proven production worthy. The requirements to perform chip ID are:

- An approximate 200x200 micron area of each die for the placement of the chip ID grid.
- A single field of one product reticle in a set dedicated to chip ID (punch field).
- An Ultratech 2000 Series stepper with chip ID machine code.

The overall process throughput, overlay and resolution of the chip ID layer, and impact to reticle cost and production are minimally effected.

This technology innovation extends failure analysis tracking and inventory control to packaged chips. It enables access to the complete processing history of the chip, including batch number, wafer number, and chip position on the wafer, as well as other items of interest to the semiconductor manufacturer.

9. Acknowledgments

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10. References

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