

A Low Cost Lithography Process for Flip-Chip Applications in Advanced Packaging Industry

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Although flip-chip solder bump technology has been practiced for over 30 years, it is only now on the verge of making its way into mainstream packaging. Array packages are becoming very popular due to their inherent advantages in interconnect density, electrical performance, speeds and chip size. The number of pin counts for advanced microprocessors, controllers and ASICs is outgrowing the limitations of wirebonding, and future I/O (Input/Output) counts of up to 3000 or even 5000 will only be realized by using array type bonding.

The traditional solder bump technology requires a shadow mask for the evaporation process. The drawbacks of this technology include inefficiency of evaporating thick metal, inferior critical dimension (CD) control and issues related to disposal of the shadow mask.

Newer technologies employ electroplating, which uses an imaging step into thick resist or Riston. This step opens bump areas over the pads where the resist acts as a blocking layer. The step is also used as a means to control bump height in the subsequent plating process.

This paper presents a low cost thick resist manufacturing process that meets bump bonding technology requirements. SEM cross-section micrographs show a greater than 1:2.8 aspect ratio in thick resists (greater than 25 μm). This paper also shows that key lithography tool success factors are high throughput, high wafer plane illumination intensity, low cost reticle technology and a pattern recognition based alignment methodology.

1.0 Introduction

As in any other sector of the semiconductor industry, the electronics packaging industry is driven by the demand for packages that are 'smaller, faster, cheaper.' The better electrical performance and higher number of I/O (Input/Output) counts available using solder bump area array packages have aroused semiconductor manufacturer's interest throughout the world.

The solder bump interconnection or "flip-chips" technology was first proposed by IBM in 1964 to eliminate the expensive, unreliable and low productivity manual wire bonding process. Later on,

the Controlled Collapsed Chip Connection (C4) was introduced [1, 2, 3]. Since then, IBM has made billions of chip-to-substrate solder connections using this technology with excellent results. Many other companies have also modified and extended this technique, but the concept remains essentially unchanged [3].

A low cost manufacturing process for bump features is required for flip chip technology to be widely accepted in the semiconductor industry. Traditionally, the bumps were created using vacuum evaporation. A molybdenum mask was aligned and clamped onto the device wafer. Bump metals were then deposited by evaporation onto the wafer through the metal mask [2]. This process is illustrated in Figure 1.

Disadvantages of the evaporation technique include high per wafer costs, alignment difficulties and accuracy, wafer contamination, expensive mask costs, poor bump diameter control and metal mask disposal problems after evaporation. As metals are deposited on the metal mask, it has to be etched away after each evaporation. The bump holes were enlarged each time and the whole mask has to be discarded after a few etches.

Another approach is to rely on thick film lithography and electroplating techniques. The wafers are first sputtered with a thin seed metal layer, barrier metal (TiW) and gold (Au), after exposing the passivation on the metal pad layer. Wafers then undergo a photolithography step to define the window for the electroplating bump metals (Au or Pb/Sn). After electroplating, the thick resist and the seed metal layer are removed leaving the bumps behind. The bump is then reflowed in an inert atmosphere to form approximately hemispherical bumps [4, 5]. This process is demonstrated in Figure 2.

2.0 Lithography Tools in Bump Processing

Most current low volume and development efforts on bump processing have relaxed requirements for overlay and resolution and therefore allow for use of less sophisticated exposure tools. Nowadays, the trend for high volume, high yield bump processing is resulting in tighter requirements. Fully automated stepper processes are becoming the standard in this industry.

2.1 Proximity Printers

Highest volume use in bump processing so far has been proximity printers, since their initial capital cost is low, and the processes were fairly unsophisticated: 10 μm resolution, overlay measured in mils, thick resists with long exposure times requiring up to 2000 mJ/cm^2 and low level of automation with typically manual align.

Since these tools expose an entire wafer at one time, exposure times of 30 to 60 seconds—in addition to the manual align are common. Since the irradiance decreases as a square function of area, processing of 150 mm and now 200 mm wafers has made these tools uneconomical.

Based on the SEMATECH Cost of Ownership (CoO) model, a generic analysis is shown in Figure 3. This analysis compares the five year cost of ownership between a traditional proximity lithography tool and a high throughput lithography stepper for a bump operation line. The result clearly shows that the high throughput, low reticle cost and high reliability offered by the stepper allows a lower cost solution for packaging.

Also, since proximity masks are 1X masters, 150 mm wafers require 7.25 inch masks and 200 mm wafers the non-standard size of 9 inch masks. Mask costs have risen over the past few years and write times are still the controlling factor for overall mask cost (larger write area = higher cost). Nine inch substrates are expensive and also difficult to obtain. Job-decks for these proximity masks are based on full wafer arrays and need to be generated from the complicated stepping arrays, matching the steppers columns and rows commands and array origin offsets. Overall the proximity process is complicated and prone to errors.

To process 200 mm wafers, photo limited yield becomes one of the most significant considerations. Since proximity printers operate at very close gaps of 20 to 100 μm (depending on the required contrast), tight control of the gap distance needs to be maintained. Any contact of mask and wafer creates defects, not only on the wafer currently in process but also on all subsequent wafers due to residuals building up on the master mask. Frequent cleaning of the masks also limits their lifetime. Die losses due to printing defects are very costly at this stage, since the wafer is completely processed. This is especially true for high end products with large area die that are subject to high dollar yield impact, since the defect density/area could potentially damage a lot of die causing a large revenue loss.

Certain alignment schemes require upfront removal of thin film stacks covering global alignment targets, but even if this is not required, valuable wafer real estate needs to be reserved for global manual alignment. Fully automatic wafer alignment requires at least the same global alignment, compensating for some of the X and Y translation and $Y_1 Y_r$ rotation, but no scaling adjustment can be made. Runout and die rotation will cause misalignment of the bump, with at least some performance loss, if not long term reliability problems. Mismatch of wafer array and 1X Master bump mask can be compensated to a certain degree, but any mistake in the job-deck layout for these masks is costly and causes delays in final delivery schedules.

Resolution limits for redistribution layers might also approach the 2 μm or below critical level, so that the proximity systems would be forced to go into a soft contact mode which will increase the risk of mask contamination and repeating defects.

2.2 Reduction Steppers

The use of reduction steppers in this application is very limited. Although most of the manufacturing process will be based on lithography using DUV i-line or g-line reduction systems at least for the critical process steps. The backend processing has problems employing these tools

due to their limited depth of focus—especially in thick resist applications of 20 to 50 μm or more—and their low wafer plane irradiance.

Schemes to work around some of these complications are problematic. The high exposure energy requirements cause extremely long exposure times, subjecting the lenses to excessive heat. The heat cycles are so high that the magnification control mechanisms have to be disabled by either shutting down the lens controller or mag correction lens. Damage to the lenses, especially by degrading the optical coatings, might be possible.

Focus ‘drilling’ by using ‘flex’ or other reported schemes for multiple focus settings per exposure field are further limiting the low throughput (in some cases less than 10 wafers/hour), and will only work up to a certain resist thickness.

Other reported problems include “haze” or excessive stray light within the lens [6] due to the high number of elements. In the worse case, even printing of peripheral reticle data (bar-codes, logos and fiducials) have been seen, despite accurate blind setting accuracy of the reduction stepper.

Employing “older,” fully depreciated steppers in this arena still causes most manufacturers problems with matching the field sizes and in some cases the alignment scheme since most of these tools have some sort of laser “scatter” alignment technique. Edge detection will be difficult due to the planarizing thickness of the resist and the underlying roughness of the pad metals and passivation layers. Low light levels from the backscattered signal will further complicate any alignment signal detection.

A vision based alignment system, like that currently being used for most back-end packaging equipment (dicing saws, pick-and-place bonders, inspection equipment, etc.), has not been incorporated in any of the leading edge reduction stepper manufacturers’ tools.

2.3 Lithography Tool of Choice

An Ultratech Titan Wafer Stepper[®] was the exposure tool of choice for this application. This stepper is based on the patented 1X Wynne-Dyson lens design using broadband g- and h-mercury lines including the wavelength continuum from 390 to 450 nm [6]. This is a very efficient optical design that consists of five optical elements and delivers very high intensity light at the wafer plane. It has a numerical aperture of 0.26 and a partial coherence of 0.6, which suits it well for thick photoresist or polyimide applications [7, 8]. The combination of the simple optics design and broadband exposure spectrum allows for a very high wafer plane intensity. This particular capability enables high throughput even under high dosage exposure conditions that are usually associated with thick film lithography.

Although no alignment is required in this experiment, this stepper is equipped with a pattern recognition based alignment system called Machine Vision System (MVS). The MVS alignment system allows auto-alignment using almost any unique existing feature on the wafer as the alignment mark. This capability greatly enhances the effectiveness of the tool for this application

and alleviates the burden from the end-user to make special dedicated alignment marks on the wafer.

3.0 Experimental Method

Shipley MICROPOSIT®SJR®5740 photoresist was spun on the wafer using a Solitec Manual Coater. A double coating was applied on the wafer to achieve a final film thickness of 28 μm. Hot plate softbake at 100 C° for 180 sec was applied after each spin and a cool down period of 15 minutes was allowed in between each resist spin. The film thickness was measured using a Prometrix FT700 film measurement system. The detailed coating process is outlined in Table 1.

Process Step	Equipment
Vacuum bake, HMDS vapor prime	YES LP-3 Oven
Manual dispense 10 ml Shipley SJR® 5740 photoresist	Solitec Manual Coater
Six second spread at 1000 RPM	Solitec Manual Coater
Thirty second spin at 1700 RPM	Solitec Manual Coater
Hotplate softbake at 100 C° for 180 seconds	MTI Flexifab Track
Cool down 15 minutes	
Manual dispense 10 ml Shipley SJR® 5740 photoresist	Solitec Manual Coater
Six second spread at 1000 RPM	Solitec Manual Coater
Thirty second spin at 1700 RPM	Solitec Manual Coater
Hotplate softbake at 100° C for 180 seconds	MTI Flexifab Track

Table 1: Photoresist Coating and Softbaking Conditions

Wafers were then exposed on an Ultratech Titan Wafer Stepper at dosages of 1500, 1800 and 2000 mJ/cm². Wafers were developed for 10 minutes in Shipley MICROPOSIT®454 undiluted developer. An immersion develop process was performed in a round container with constant circular agitation.

4.0 SEM Results

Figure 4 shows a very clean pattern with straight wall profiles of 10 µm contact holes and lines/spaces in 28 µm thick resist. Figure 5 shows two additional line/space SEM micrographs that show excellent 20 µm line/space openings at a 20 µm pitch. The one on the left hand side was exposed with 2000 mJ/cm² at -15 µm focus bias while the one on the right hand side was exposed with 1500 mJ/cm² at +15 µm focus bias. After the windows are successfully defined, the wafers can be electroplated to give either mushroom shaped bumps or straight wall bumps, depending on the application.

5.0 Conclusion

As the need for larger number of pin counts, higher interconnect density, better electrical performance, faster speeds and smaller chip size grow, the packaging industry needs to develop new and more cost effective solutions to meet these requirements. This paper has shown that photolithography can provide the technical capabilities to manufacture bumps that are essential in the flip-chip and other advanced packaging technologies.

In order to fully realize the advantage of photolithography for the advanced packaging industry, a low cost manufacturing process has to be developed. This paper has shown that the success factors of a photolithography tool for this application are high wafer plane intensity, high throughput, high reliability and machine vision system for auto-alignment. We have shown that a commercially available stepper can provide all these success factors and that a low cost manufacturable process can be developed.

The SEM micrographs show that a 1:2.8 aspect ratio for over 28 µm thick film process is achievable. A Cost of Ownership (CoO) analysis confirms that this process can provide the lowest manufacturing cost for the bump application.

6.0 References

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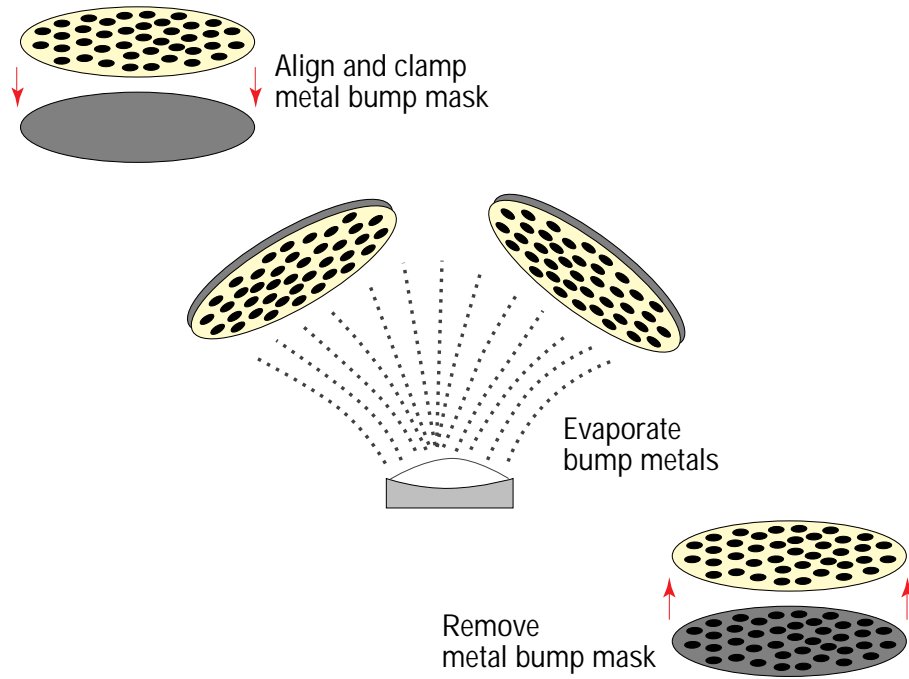


Figure 1: Evaporated bump process using metal mask.

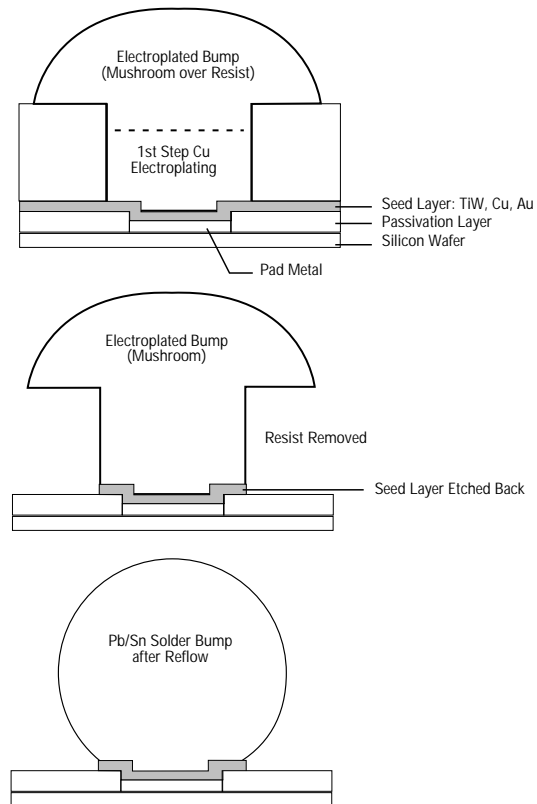


Figure 2: Electroplated bump process using photolithography technique.

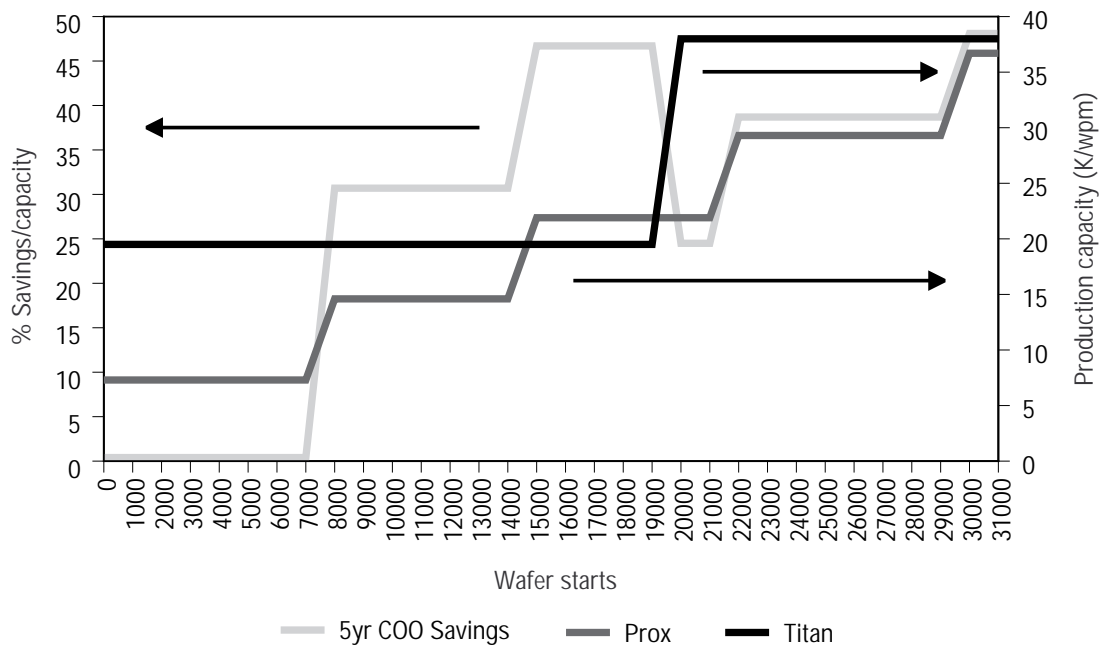


Figure 3: Year cost of ownership analysis results comparing proximity aligner and 1X high throughput stepper.

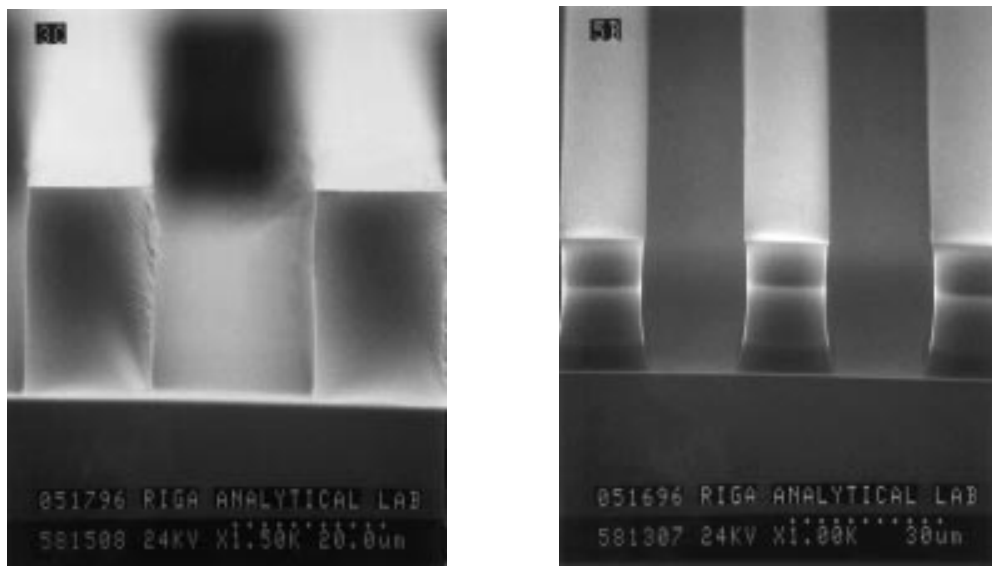


Figure 4: SEM micrographs of 10 um contact holes and lines/spaces in 28 um thick resist.

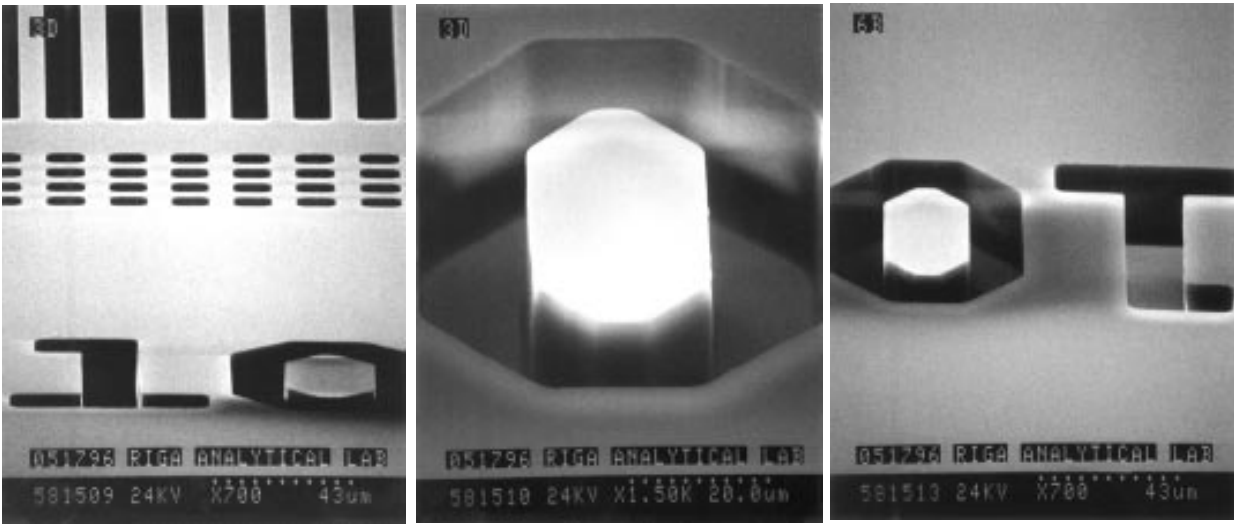


Figure 5: SEM micrographs of 20 um lines/spaces openings at a 20 um pitch in 28 um thick resist.