Photolithography Challenges for the Micromachining Industry

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1.0 Introduction

Micromachining can be considered a fabrication technology for building devices with feature sizes from a few microns to a few mils, often with moving parts. MicroeElectroMechemical Systems (MEMS) is a term often used interchangeably with micromachining. MEMS devices, however, are distinguished from micromachining by their mechanical nature, because moving parts are often a required component to enable them to sense or manipulate the external environment.

2.0 Micromachining Applications

The ability to create moving parts on a miniature device immediately opens up applications for both sensing devices and devices that physically exert force to create motion. Devices in these two categories are classed as sensors and microactuators, and they comprise virtually all of the current micromachining applications. Sensor applications that dominate today’s micromachining products are being built for nearly all of the major market segments. The automotive industry has become the primary user of micromachined devices with applications including speed sensors, accelerometers, and temperature and pressure sensors.

The two micromachining applications that have found widespread use are accelerometer devices (primarily for airbag deployment sensors) and pressure sensors for automotive, industrial control, and biomedical markets. Both of these fit the definition of MEMS devices with moving or flexing structures.

Accelerometer devices typically use capacitive sensing to measure dynamically the capacitance developed between a moveable surface and a fixed surface. As one surface moves away from the other, the capacitance changes, and movement is sensed.

Pressure sensor devices are manufactured by etching the back side of a silicon wafer leaving a membrane and creating a cavity, and then embedding a sensor in the top of the membrane to identify any movement. The sensor could be capacitive, as in the accelerometer, or a strain sensor

as in a diffused resistor. The silicon wafer is then bonded to a thicker substrate, with the cavity either sealed or open to the atmosphere (see Figures 1 and 2).

3.0 Fabrication Technology

The foundation of micromachining is the Microelectronics Industry with its extensive semiconductor fabrication technology. Because the critical dimensions of MEMS devices are approximately the same as transistor fabrication, the material and process understanding developed over the decades in semiconductors is directly applicable to micromachining.

The current micromachining devices have an advantage over an equivalent semiconductor counterparts. The critical dimensions driving the pattern transfer process are nearly an order of magnitude greater for MEMS than those for transistors. This allows the fabrication of MEMS devices to fit into the start-up budgets of the classic entrepreneurial channels.

Two divergent approaches for generating device structures involve surface layering and etching and deep silicon etching. The former is referred to as surface micromachining, and the latter is called bulk micromachining. These approaches differ both in terms of the ease of manufacturing and in terms of the performance of devices built using these techniques.

4.0 Lithography Requirements

The need for pattern transfer is an inherent part of the micromachining fabrication process. With the dimensional feature size requirements approaching a few microns, photolithography approximating semiconductor standards becomes a key process requirement. Because the demands of the microelectronics industry are covered in many other publications, this article will focus on those areas where the demands of micromachining differ significantly from semiconductor requirements.

The challenges in pattern transfer for micromachining are driven by the significant differences in topological of many of these devices. For example, many devices are built on a dielectric layer, that is later undercut for freedom of motion. Others are isolated by being built over a cavity. The separating layer is broken through to leave them nearly freestanding. The challenges center around both the prominent role that etching plays in creating the structures and the need to pattern across surfaces that vary significantly in height (sometimes over many tens of microns). These challenges can be viewed by their impact on resist and imaging technology. Table 1 summarizes the major issues involved.

	Resist Challenges	Imaging Challenges
Topography	**Step Coverage** Resist integrity over significant steps	**Depth of Focus** Quality images over significant steps
	Thickness Uniformity Thickness control on varying topography	**CD Control** Linewidth control across significant topography
Pattern Transfer	**Etch Resistance** Resist integrity under aggressive etch conditions	**Image Quality** Quality images through thick resist
	Adhesion Resist adhesion to prevent undercutting	**Resolution in Thick Resist** Step edge profiles for fine geometries in thick resist

Table 1: Summary of Resist and Imaging Challenges

5.0 Resist Technology

The challenges associated with resist technology for coating and pattern transfer are driven by the resist's ability to accomplish the following:

- Uniformly coat the substrate
- Adhere to the substrate layer
- Withstand the pattern transfer etch process.

The ability of the coating techniques to provide high quality pattern transfer across significant topography is very dependent on the uniformity of the resist coating that is achievable. One of the difficulties that arises with structured devices is the effect that topography has on the ability to provide uniform resist coatings during subsequent processing steps. The problems introduced typically impact the uniformity of critical dimensions (CD) and vary depending on the extent of the topography and its position on the wafer.

The step coverage issues address both the ability of the resist to stand up to the etching process and the ability of the imaging tool to provide controllable pattern linewidths over major topography changes.

Substrate format issues also can effect the uniformity of the resist thickness, because similar problems may occur if square rather than round substrates are used. The normal spin technique for photoresist distribution across the substrate generates nonuniform thickness patterns at the substrate corners, which can effect CD uniformity during the imaging step. Industries that use square substrates, such as the Thin Film Head industry, require special techniques for improving the resist uniformity at the corners. Fringe-free coating techniques have been developed for the photoresist application process, but some of these make the overall thickness uniformity harder to control. An equivalent problem arises when the topography of the MEMS devices is sufficient to cause localized resist flow perturbations [1]. This shadowing during resist spinning will effect the adjacent structures within the shadow distance. Unfortunately the effect on the neighboring structure will vary depending upon its radial direction from the center relative to the topography (see Figure 3). Besides effecting the CD control of the neighboring devices, this can introduce what appear to be scaling shifts due to apparent displacement of the alignment marks.

The thick resist requirement may come from the need to protect the device during an aggressive etch pattern transfer process (illustrated in Figure 4). Reactive ion etching (RIE) has become a popular method of etching significant dimensions into silicon for bulk etched devices. This etch process allows etching device structures several hundred microns into the silicon substrate; during the etch process, the unetched surfaces must be protected by resist thick enough to withstand the prolonged erosion of the etching process. Thickness ratios of 10:1 to 50:1 (silicon etched versus resist eroded) have been demonstrated with various etching processes. To etch a 200 mm groove under these conditions would require a resist thickness of from 4 to 20 mm, depending upon the etch process available. The choice of resist is also important for maximizing the etch resistance under the aggressive etches required in creating the topography for MEMS, but those choices must be weighed against other lithography characteristics and manufacturing costs (see Figures 3 and 4).

Depending upon the underlying layer material and the lateral challenge of the etching process, the adhesion of the photoresist to the substrate may play a critical role in achieving a reliable pattern. Adhesion promoters are often used to optimize against difficulties at this step.

6.0 Imaging Technology

The primary challenge to imaging technology involves the variation in surface topography on some devices. Many of the imaging challenges are addressed by providing an adequate aerial image throughout the topography variation.

The numerical aperture of the lens and the wavelength of the illumination are important to the optical transfer function. The resolution and the depth of focus are related to these parameters, which are defined at the Rayleigh limits in the following manner:

$$R = (k_1,\lambda)/NA$$

$$DOF = \pm (k_2\, \lambda)/NA^2$$

where R is the resolution, k_1 and k_2 are k factors, λ is the wavelength, NA is the numerical aperature, and DOF is the depth of focus. The k factors are defined in the practical use of these relations (determined empirically for the lithography process in use).

Depth of focus for the imaging tool, as well as other focus compensating techniques, is typically used to maintain the pattern fidelity across the topography. The current resolution requirements for micromachining tend to lag the semiconductor requirements by nearly an order of magnitude. This makes possible the design of imaging tools that can provide production level reliability with impressive depths of focus.

The key capabilities for successful lithography are to:

- Identify the resist surface and place the aerial image appropriately into the resist layer to achieve the maximum pattern transfer fidelity
- Compensate for variations in topography of the imaging surface in order to provide optimal image transfer to all critical device areas
- Transfer the pattern to latent image within the resist as efficiently as possible to maximize production throughput.

One advantage of stepper technology is its ability to adjust to variations in the pattern placement of previous layers. The keys to success here are site-by-site alignment and sophisticated focus routines. The solutions to many of the issues arising in the Thin Film Head industry are directly applicable to MEMS devices. One of the techniques developed to create optimum image transfer in thick resist is focus drilling [2]. This technique involves adjusting the total image dose across a series of flashes with different image intensities being exposed at different focus depths. This technique can be used to control the resist wall profile carefully after develop, enhancing the critical performance of the image transfer.

A technique used to identify the resist surface is to measure the back pressure on a set of air probes placed around the imaging area. Algorithms have been developed to sample and identify local tilt variations in substrate or device topography for optimum pattern transfer.

One challenge is imaging through very thick resist (5 to over 50 μm), which is required to provide adequate etch protection. This thick resist requirement may stem from the topography demands, which end up depositing thick resist in topological valleys where a critical image is required. An example of this is thin film head applications that provide the read/write components to the disk drive industry. By the time the coil stack has been fabricated the final magnetic pole element (1 to

2 μm) must be imaged in the +10 μm of thick resist that has pooled into the area adjacent to the coil structure. Because the final dimension of the pole is critical in providing the disk density performance, this challenge has a very significant impact on the manufacturing yield (see Figures 5 and 6).

As in the case of a thin film head coil structure, or metal line definition in large scale microprocessors, the step coverage of the resist as it attempts to coat across the corner of a steep slope is an important parameter in the success of the overall process. The greater the need for protection (for example, during the subsequent etching process), the greater the required integrity of the resist crossing the step.

As an example of extreme cases, some MEMS devices need components defined at the bottom of a cavity. The depth of the cavity could be several tens of microns. This requirement combines both resist and imaging difficulties; a uniform resist coating down the side of the wall slopes (as well as on top and in the cavity) needs to be provided, and the pattern must be acceptably imaged along those surfaces. The use of an electrodeposited resist (such as PEPR 2400 from Shipley [3]) makes the radical departure from spin coating needed to address these difficulties. Multiple focused exposures, or in some cases reticle exchange for imaging at the cavity bottom, can address some of these imaging difficulties.

7.0 Manufacturing Issues

Key elements of manufacturing success are high throughput and yield. To accomplish these, a lithography tool must provide high wafer plane intensity, rapid substrate handling, and low defect density. With its ability to step defect-free images across the substrate, stepper lithography came to dominate the semiconductor industry by offering the high yield solution to pattern transfer. As critical dimensions shrink and manufacturing volumes rise, this solution will see widespread use in micromachining fabrication as well. MEMS manufacturers can use low cost, high productivity steppers being used in commodity semiconductor fabrication, avoiding the steep price of steppers designed for advanced semiconductor applications.

8.0 Summary

The commercialization of the micromachining market is still in its infancy. Microlithography, adapted from the semiconductor industry, has found a critical place in the fabrication of MEMS devices. The constraints on this technology are often related to the varying topologies resulting from fabricating three-dimensional structures. Thickness control of the photoresist layers is one of the principle challenges for these structures.

Thick resist is often needed as part of the device fabrication requirement, either for plating tall structures or for erosion protection during etching. Some of the key requirements for successful lithography tools are:

- Use of a flexible handler capable of processing bonded wafers
- High wafer plane irradiance for efficient thick resist image definition
- Precise pattern placement for critical overlay imaging
- Noncontact imaging for high production yields
- Defect-free reticle printing for high device yields
- Use of a wide variety of resolutions and depths of field.

Manufacturers of many of the current devices in the sensor market could gain performance and manufacturing advantages by scaling down and employing higher levels of integration. Photolithography will be key to progress in this area. As micromachining companies accelerate products into the marketplace, microlithography imaging tool vendors must be responsive to the needs of this growing industry.

9.0 References

1. White, L.K., "Characterization and Simulation of Spin-Coated Resist Contours," SPIE Vol. 539, p. 32.

2. Fukuda, H., Imai, A., Okazaki, S., "Phase-Shifting Mask and FLEX Method for Advanced Photolithography," L.K. SPIE Vol. 1264, Optical/Laser Microlithography III, 1990, p.14.

3. Linder, S., Baltes, H., Gnaedinger, F., Doering, E., "Photolithography in Anisotropically Etched Grooves," IEEE Ninth Annual International Workshop on MicroElectroMechanical Systems, Feb. 1996 , p. 38.

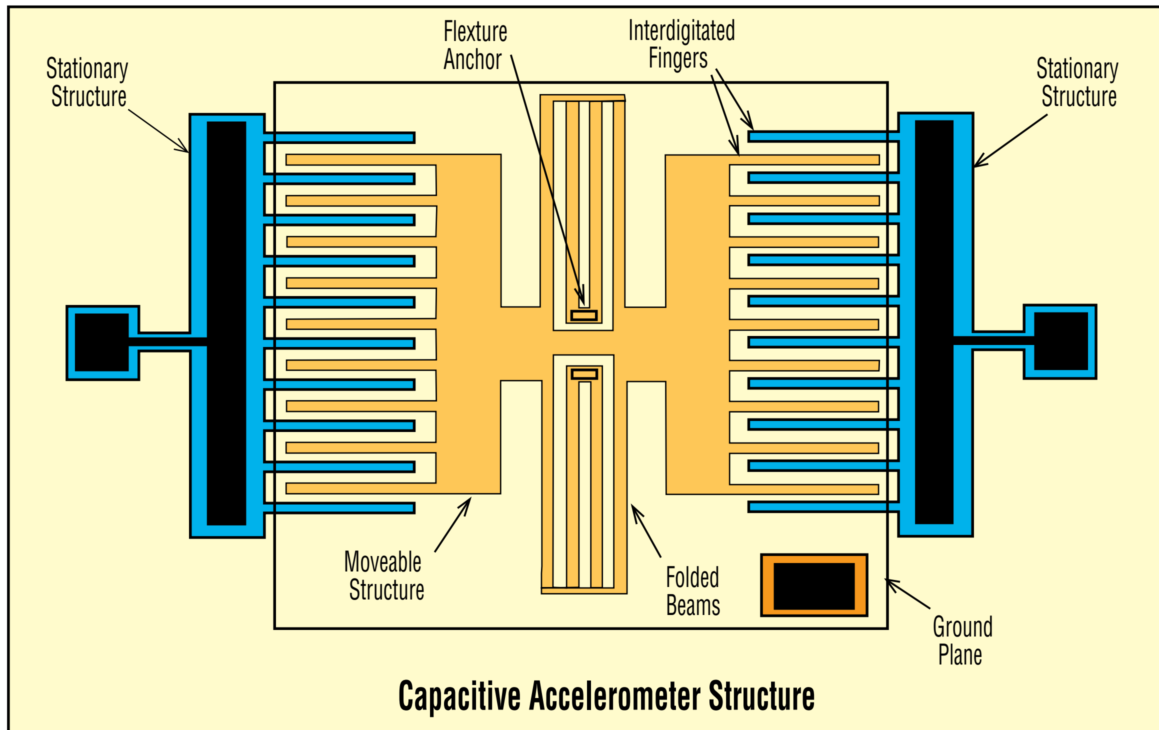

Figure 1: Capacitive Accelerometer Structure

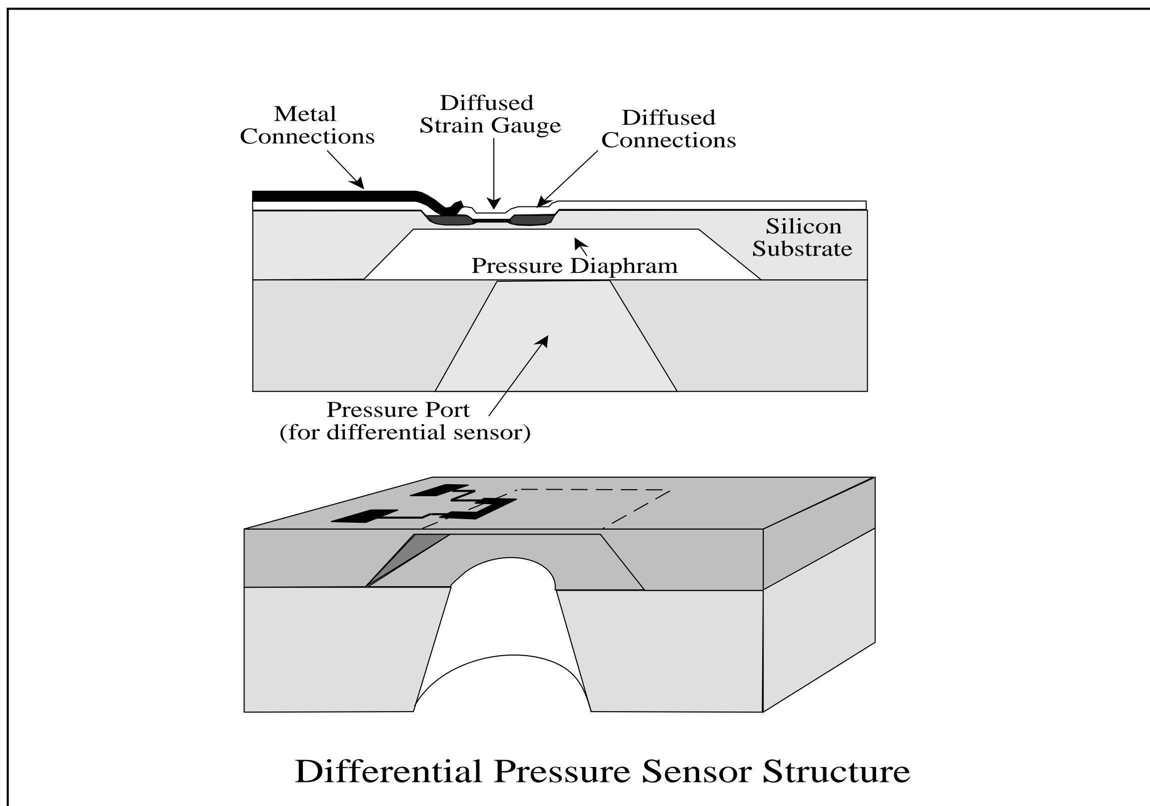

Figure 2: Bulk Etched Pressure Sensor Structure

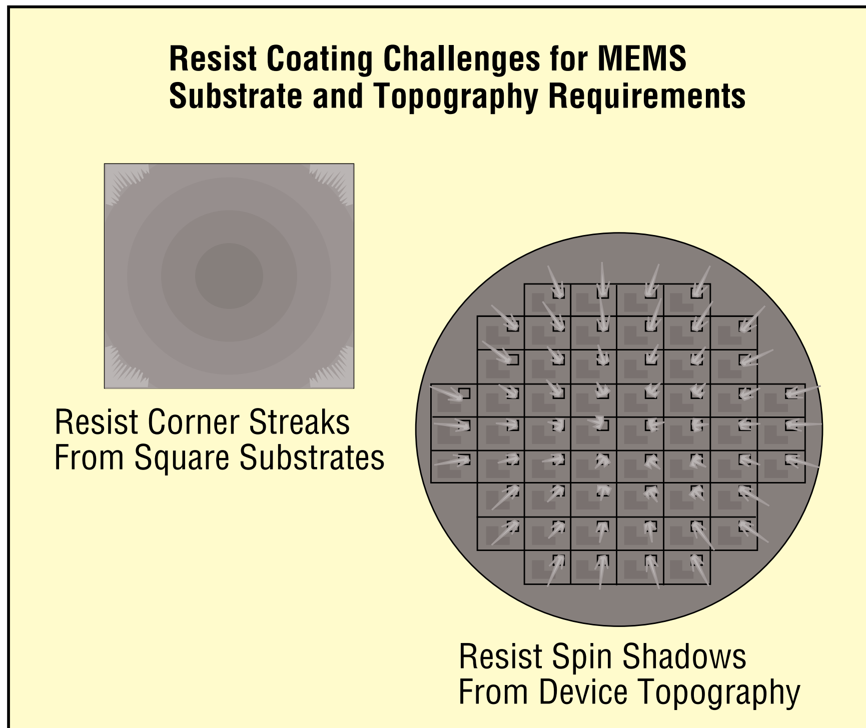

Figure 3: Resist Coating Challenges

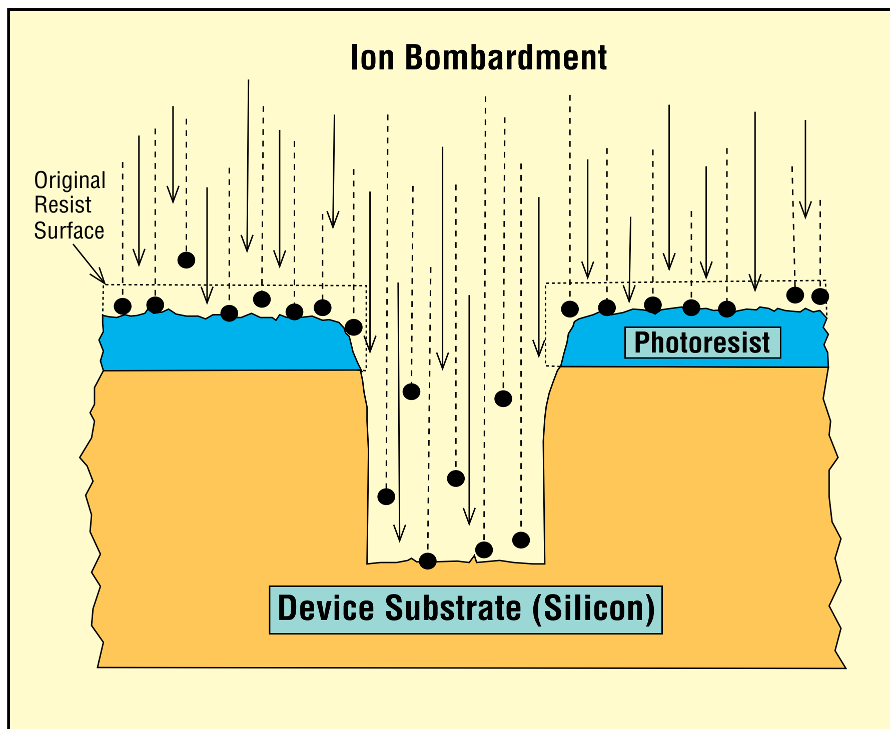

Figure 4: Integrity Challenges for RIE Etching

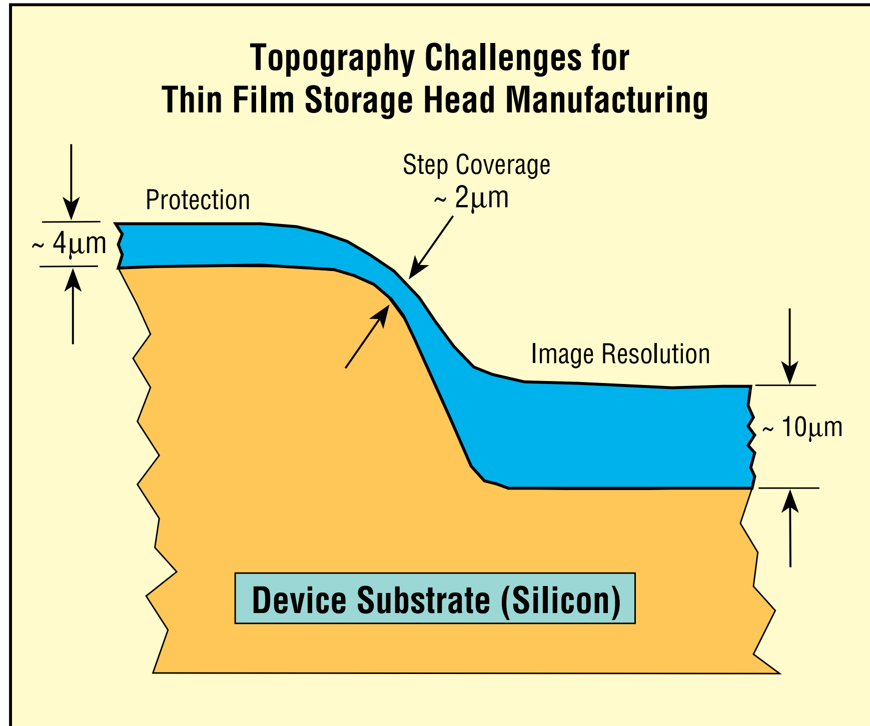

Figure 5: Topography Challenges in Thin Film Heads

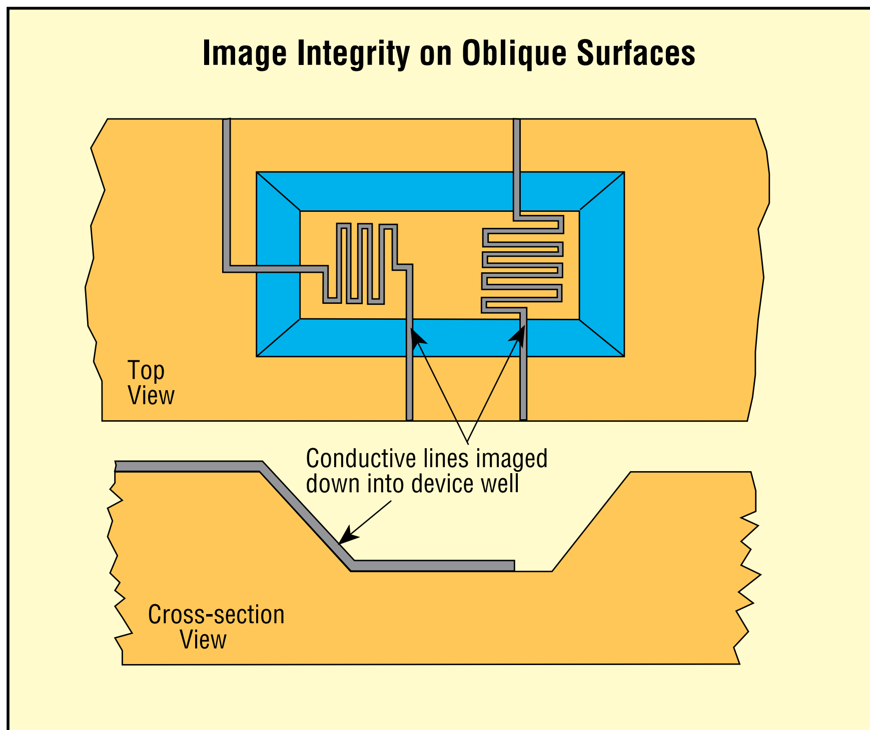

Figure 6: Image Integrity into Cavities