Imaging and Resist Technologies for the Micromachining Industry

David Craven
Ultratech Stepper, Inc.
San Jose, CA 95134

1.0 Abstract

Pattern transfer and process layering sequence constraints determine what practical three-dimensional structures can be micromachined. Three important interdependent technologies determine the limitations that bound device design.

- Resist and coating capabilities (predefinition)
- Lithographic image capabilities (structural definition)
- Structural creation through etching or plating (pattern definition)

The two primary challenges to device pattern transfer are high aspect ratio and high topography requirements. These two structural challenges come out of the interdependent technologies mentioned above. This paper reviews these challenges as well as possible solutions that are being investigated.

2.0 Introduction

The purpose of this paper is to review the pattern transfer issues that pose challenges to micromachining design and manufacturing as well as their possible solutions. The motivation for this work is the critical nature of lithography as a technology that enables the advancement of the micromachining industry.

The major steps in the pattern transfer process will be identified and used to explain the individual aspects of the challenges involved with high aspect ratio and high topography. The structural perspective of micromachined devices will then be introduced as a foundation for identifying the high aspect ratio and high topography challenges. These two key photolithography challenges will then be discussed.

A useful perspective is to view micromachining applications by the structures used to create micromachined devices. Although these structures could be classified by their physical

configuration, it is sufficient at this level to identify the basic three fabrication regimes used to build devices.

- Monolithic structural growth
- Surface micromachining
- Bulk and deep etch micromachining

Monolithic structural growth is typified by plating applications, where monolithic and often high aspect ratio structures are grown on the substrate or adjacent layers. Surface micromachining, on the other hand, results from numerous relatively thin layers used to form structures often all across the surface of the device. The bulk fabrication approach creates structural components down into the substrate, in some cases connecting all the way through the substrate into buried cavities. Clearly the fabrication challenges can differ significantly depending upon which of these approaches dominates the device design.

3.0 The Micromachining Pattern Transfer Process

Structure is what differentiates micromachined devices from other miniature components. The device designs and hence the applications that can be realized with this technology are limited by type and range of structures that can be created. The pattern transfer process used to create the structural components has ramifications all the way through to the achievable product performances.

Lithography is the primary enabler in the pattern transfer process. The ability to create the final pattern in or on the substrate results from the ability to map the image pattern into the substrate. If the Micromachining industry is to continue to expand to its full potential, serious work must be done to further develop resist and imaging capabilities.

3.1 Process Steps

The process of creating structure in a micromachined device can be broken down into four discrete sections, as described in the Table 1. Each of these exhibits strong dependencies on the adjacent sections. Achieving real process capability requires understanding the various sections and their dependencies.

Predefinition	Pattern Definition	Structural Definition	Structural Completion
Substrate Preparation	Lithography Patterning	Etching	Definition Material Removal
Mask/Reticle Creation		Plating	Mold/Support Release

Table 1: Components of the Pattern Transfer Process

Predefinition

Predefinition refers to the activities that take place before the imaging step. Activities such as substrate preparation (adhesion promotion) and photoresist application are included here. The creation of the reticle could be included here as well.

Pattern Definition

The second component of the pattern transfer process is pattern definition. This is primarily the lithography step where the mask pattern is imaged in photoresist prior to pattern transfer into the substrate. This step in the process is the primary subject of this paper.

Structural Definition

Structural definition describes the step that actually creates the structure. Here the image pattern is transferred to the substrate resulting in a physical structure. Two principle forms of patterning definition are plating and etching.

Structural Completion

Structural completion refers to the finishing steps needed to complete the pattern transfer. These activities include removal of the definition material (such as photoresist), structural release (undercutting the oxide), and various antistiction process steps. Although the structural completion steps are important to a fully functional micromachined device, they do not relate to the central issue of this paper and hence will not be addressed.

3.2 Challenges to Pattern Transfer

Micromachining structures exhibit a wide variety of physical properties within an extremely broad collection of sensors and actuators. As a result, an incredible variety of structural demands arise in the formation of sensor and actuator products. The pattern transfer challenges are likewise very broad, but there are common challenges that continue to come up in many of the various applications, which makes them worth addressing [2]. The two most prominent challenges are high aspect ratio and high topography.

The approach that will be taken here is to review the issues and possible solutions in the first three pattern transfer process steps for each of these challenges. Thus, high aspect ratio and high topography will be examined by process step: predefinition, structural definition, and pattern definition. The issues arising in each of these process steps will be reviewed and some of the techniques that are being developed will be discussed.

Throughout this paper, various types of structures and devices will be used to exemplify the issues. These will be particularly relevant in discussing high topography issues. Many references will be made to issues in the Thin Film Head (TFH) storage media industry because of TFH devices, similarity to MEMS devices [4, 5].

4.0 High Aspect Ratio Structures

High aspect ratio structures come in two varieties: those that are built above the substrate surface (typically by plating processes) and those that are etched into the substrate (often by deep reactive ion etching).

4.1 Plating Applications

For plating applications, the quality of the final structures is often dependent on the capability of the available plating mold material (resist) to achieve both high aspect ratio configurations and quality sidewall profiles.

The range of aspect ratios that can be achieved under conventional processing varies with the exposure energy. For conventional ultraviolet (UV) exposures, aspect ratios between 3:1 to 5:1 are achievable. This is in sharp contrast to the aspect ratios of 50:1 to 100:1 demonstrated from high energy (synchrotron) radiation. Besides this and the initial capital investment required for synchrotron radiation sources, there are many other application constraints that differentiate these two approaches. This paper will concentrate on conventional UV radiation exposures.

4.2 Deep Silicon Etch Applications

For deep silicon etch applications, the quality of the final deep etch structures relies on the reactive ion etch (RIE) processes available, the geometry of the device, the materials and etchants being used. This is an extension of the basic pattern transfer capability, and much work is being done to further develop RIE. Many applications could derive enhanced performance by adopting this process. The aspect ratios that are achievable with deep silicon RIE range between 10:1 and 20:1 for practical applications.

The challenge that deep silicon etch presents for pattern transfer depends on the selectivity between the etch mask and the substrate material. Typically the etch mask material is photoresist

or silicon dioxide. The typical selectivity ratios for photoresist are between 40:1 and 80:1. For an SiO_2 RIE process the ratios are between 70:1 and 300:1.

As an example, if a 300 µm deep trench were to be etched in silicon with a photoresist mask whose selectivity ratio is 50:1, a photoresist trench of 4.3 µm would be required. However, if an SiO_2 layer were used as the etch mask material for the same etching requirement, only 1 µm of oxide would be needed. Only a thin layer of photoresist would be needed to etch the oxide and provide this capability.

5.0 High Aspect Ratio Challenges

The primary lithography challenge for high aspect ratio micromachined structures is achieving sufficient depth of focus from the lithography tool. This is governed by the need to extend the uniformity of the aerial image as far into the resist as possible. This is important in order to produce quality images with good critical dimension (CD) control and sidewall profiles.

Different applications have different aspect ratio requirements depending on the total volume or mass of the residual structure. In the case of capacitive sensors, close parallel sidewalls provide high performance. If the process technology is surface micromachining, the required aspect ratios may not be that great. However, for an accelerometer built with deep silicon RIE for maximum mass, the aspect ratio may become quite challenging. On the other hand, if the application were to create microfluidic fluid channels, a very low aspect ratio may easily suffice.

For plating applications, the plating process also places special demands on the mold material (typically photoresist), subjecting the retaining walls to different pressures and temperatures. The choice of resists, substrate surface preparation, as well as curing steps must all be taken into consideration to develop a successful process.

The choice of material for the high aspect ratio structure must be selected based on performance, ease of manufacturing, and ease of structural integration. For deep etch structures, silicon has several mechanical material advantages as well as being easily integrated electronically.

There are many resist and coating issues including viscosity, elasticity, homogeneity for resist and throughput, edge effects, material efficiency, and thickness uniformity for the coating process. Figure 1 provides a visual assessment of where current technology is compared to where users would like it to be on some key coater issues [3].

5.1 Predefinition

Surface preparation is a major influence on the final pattern transfer capability through the strong correlation between final photoresist image and the photoresist thickness. Thus obtaining a homogeneous resist layer of uniform thickness is one of the most essential parameters in successful final pattern quality. However, the thicker the resist layer, the more it is subject to

variations in bulk versus surface effects, which are not as well understood [6]. Adequate modeling of the rheological effects of resist and spin dynamics for thick resist will be needed to successfully direct process improvements in this area.

The etch resistance of the resist coating also plays a big role in the quality of the final structure. Undercutting, pinhole creation, and peeling can all contribute to process control problems and final device performance. Some examination of resist application postprocessing steps has been tried to increase the process latitude in this area. The choice of etchant process can play an overwhelming role in resist erosion performance.

There are several avenues for improving performance in the predefinition area based on working with the resists or coating equipment. Unfortunately, most of this work is still in the development stage and it is too early to quantify progress.

Resist and Coater Development for Thick Resist

Adaptive stray techniques for generating thick resist layers, for example, allow a change in the dynamics of solvent evaporation. If this process can truly shift the coating process to a new paradigm, the conventional bounds on practical resist thickness may be significantly expanded. As promise is demonstrated in this area, new resist compositions may be developed to optimize the process.

Multilayer Processes

One technique is to use layers of different resists with specific characteristics and then stack these resist layers to optimize the final sidewall profile (see Figure 2). The characterization of these resists as well as the process tuning to optimize the combined stack requires a great deal of work. Only when an application demands the special advantages of such a process can the effort become worthwhile because this approach must be customized to specific conditions [4].

Contrast Enhancement Processes

Contrast enhancement resists have unique transmissive characteristics that can be used as an intermediary in transferring mask patterns to the substrate resist. These resists are layered thinly on top of another polymer and then exposed. The exposure dynamically changes the transmissivity of the contrast enhancement resist, effectively allowing a shift in the plane of the focal image. This technique is used effectively in many demanding instances, although the additional cost can be very high.

Work has been done on techniques for coating the photoresist with a thin layer of a more durable material, such as deposited oxide. With the large multiplier effect in selectivity between oxide and photoresist, this approach allows a thin resist definition process to provide an intermediate transfer to the substrate, from which a deep RIE process can finish the full substrate pattern transfer. For such a technique to provide reliable pattern transfer, the integrity of the deposited layer process must be robust.

5.2 Pattern Definition

In the arena of pattern definition, the capabilities of the imaging tools determine process boundaries. Aspects such as the numerical aperture (NA) of the optical system have a driving influence on the resolution, depth of focus (DOF), and wafer plane intensity performance of these tools.

The options for increasing the DOF of the imaging tool present various tradeoffs. The variation of DOF with NA and resolution is governed by the following equations and is illustrated in Figure 3.

$$R = k_1 \lambda/NA$$

$$DOF = \pm k_2 \lambda/(NA)^2$$

Where R is the resolution (line and space), DOF is the depth of focus, k_1 and k_2 are empirically determined coefficients, NA is the numerical aperture, and λ is the wavelength of the exposing radiation.

Since the DOF is proportional to the reciprocal of the numerical aperture squared, use of a lower NA optical system can dramatically increase the usable DOF [8, 9]. The development of the Markle-Jeong 1X array lens has allowed for systems with very low NA to be constructed and configured to scan a variable field size [10]. The extension of practical lens designs into very low numerical apertures provides a useful trade-off for much greater DOF for less aggressive linewidth requirements.

Special Focus Techniques

Special focus techniques have also been developed on standard lithography systems to extend the useful range of these tools for higher DOF applications. One such technique is called surface mapping and allows the topography of the surface to be determined on a reasonable grid size prior to imaging. This allows algorithms to extrapolate a local image plane on a site-by-site basis, which can be used to adjust for optimum focus prior to exposure.

Focus drilling is a special variation of these focus techniques. It was first developed in the late 1980s to extend the focus tolerance of an existing lithography tool and was called the focus latitude enhancement exposure technique (FLEX) [16]. Focus drilling is based on a voting scheme for distributing the exposure at a single site over a number of exposures to increase the overall quality of the image. In this case, the plane of focus is changed prior to each successive exposure, allowing the aerial image transfer to be optimally distributed into the resist. The focus drilling process is illustrated in Figure 4, along with data on statistical linewidth control gathered using this technique [11]. The exposure dose and the number of exposures can be optimized for the resist thickness and final pattern requirements.

Multilayer/Contrast Enhancement

The sidewall angle is an important parameter in determining the quality of the final high aspect ratio pattern, particularly in the case of plating applications. Detailed studies can be made to determine the sidewall angles achievable for different resist thicknesses, process conditions, exposure wavelengths, resist types, and so forth. Some specific studies of these parameters are available; however, applications usually need to be customized to meet specific needs. An example of some of the characterization work done in a recent study to investigate the variation of a Shipley cross-over resist is shown in Figure 5 [12].

5.3 Structural Definition

CD Control

Once the aerial image of the mask pattern has been transferred into the photoresist, the final structural definition must still attempt to reproduce that image with high fidelity. Erosion of the photoresist pattern during the etch step can generate a time-dependent sidewall profile that compromises the device design parameters.

Because of the nature of some plasma etches, sidewall protection may be relatively weak. This causes undercutting of the structural dimensions with etch time. Although some of this can be compensated for by bias in the mask pattern, small geometry definition could be excluded.

Etch Resistance

The ultimate depth of deep etch structures is limited by the basic nature of their process and by the thickness and selectivity of the etch masking layer. The simplest process involves using the photoresist directly as the etch mask. The thickness of the resist and its resistance to etch are the dominant factors in defining the etch depth limits available to the device designers (see Figure 6).

The ability of the resist layer to withstand the etch process is always of concern. Many techniques for resist processing and postapplication baking have been investigated to extend the available limits.

Adhesion is the other parameter that can limit the ability of a photoresist layer to deliver quality patterned structures. The surface chemistry of the layers plays a prominent role in these effects. Adhesion promoters have long been used to increase the effectiveness of coating some problematic layers, and droplet dynamics are important in this regard for spray coating techniques [13].

Resist Plating Robustness

For plating applications, the final photoresist pattern must not only have appropriate sidewall shapes, but must also be able to withstand the temperatures and stresses of the plating process. Various resist characteristics, application, and baking techniques must be developed to optimize

the final result as in Figure 7 [14]. Many of these investigations tend to be specific to the particular structure and circumstance and don't find their way into the literature.

6.0 High Topography Structures

MEMS devices are three dimensional by nature, often creating planes of structure with significant topography. Both the photoresist coating and the lithographic imaging experience major limitations when encountering structural changes of more than a few microns. Conventional spin coating equipment as well as the rheological properties of the resist material itself have been designed for planar flow characteristics. Steps, slopes or other surface variations of only a few microns exceed the boundary of design parameters for conventional coating technology. For structural topography of several microns, empirical process development is required.

The control of critical dimensions is one of the most crucial aspects of pattern definition. This parameter is largely determined by the uniformity of the aerial image across the device. The photoresist thickness varies significantly or the relative focal position or illumination intensity of the aerial image changes, the quality of the final resist pattern will suffer. Changes in topography work against the desired uniformity of that image in nearly all aspects.

7.0 High Topography Challenges

For device structures with high topography, the variations in the planarity of the surface generate multiple challenges to both predefinition and pattern definition processing. For the predefinition coating of the substrate, uniform resist thickness is the biggest challenge. For the pattern definition, three challenges arise: critical dimension control, pattern integrity across transitional regions, and quality sidewall profile definition.

Three dimensional structures of significant topography create constraints on the fabrication process flow of MEMS devices as well. Not only is the ability to transfer quality patterns in high structures with topography a major consideration, the ability to conform subsequent deposited materials to the remaining surface topography presents additional limitations.

7.1 Predefinition

<u>Discrete or Integrated Processing</u>

As part of the design methodology, the choice of discrete or integrated design must be made early. In the case of combining 3-D micromachined structures with microelectronics, many options are available:

- Multiple chip designs

- Hybrid designs (MCM)
- Flip-chip designs
- Integrated MEMS and electronics

One of the questions that arises in attempting to image patterns across surfaces with changing topography is whether to attempt an integrated image or to image different topographical surfaces separately.

Integrity of Transitional Elements

If the approach of imaging different levels separately is adopted, (for example the top substrate surface and the bottom of recessed cavities), there remains the issue of the integrity of transitional elements (such as fluid channels or electrical interconnects) as in Figure 8.

The issues of multisurface imaging and integrity of transitional elements are only just beginning to be approached. As the boundaries of pattern transfer capabilities expand in these areas, device designs will be able to develop in more productive and creative ways.

Resist Thickness Control

One of the toughest challenges in the area of pattern definition for high topography structures is the ability to coat the substrate with a uniform thickness of photoresist. Any significant topography challenges the basic assumptions needed to insure adequate resist thickness uniformity (see Figure 9). A familiar example is the discontinuity boundary at the edge of the wafer, where the surface tension and flow dynamic result in significant edge bead problems. Rheological modification of resist and spin dynamics may be required to solve this difficult problem.

Adaptive stray techniques for developing conformal coating are under investigation [3] and hold promise of some relief in this most important area.

Spin Shadowing

Likewise, structural topography generates thickness variations as the resist tries to flow over these structures. These spin shadows create two classes of problems:

- Resist thickness variations on the near and far sides of the structures can generate CD control or etch mask integrity problems.
- Directional effects of these spin shadows vary depending on the angular direction of the structures from the center of the wafer (see Figure 10).

The result is that CD variations are created in different parts of the device depending on the chip’s radial position on the wafer.

Target Migration

Alignment targets with sufficient topography can also generate spin shadows that cause an apparent positional shift during alignment. With the resist nonuniformity over the target, the optical recognition perceives an asymmetry in the target through the resist. The computational algorithms try to optimize this acquired pattern and shift the perceived center as a result.

Conformal Coating

A variety of techniques have been investigated to alleviate some of the difficulties encountered with high topography such as the use of different dwell times, spin speeds, and postbaking conditions at the resist application step to multilayering of resists of different characteristics (see Figure 11) [4].

An alternate approach is to use a spray application technique to build up the desired resist layer. The dynamics of spray coating are very different than spin coating and allow the resist layer to be built up under very different constraints. This approach is in the early investigation phase in the coater equipment industry, but results on its capabilities should be available early next year [13].

Other innovative attempts to generate solutions on high topography structures involve the use of electrodeposited resists. This approach also permits the resist layer application under very different constraints from the conventional spin techniques (for example, oblique surfaces; see Figure 12). Some investigative work with Shipley's PEPR 2400 was published in early 1996, although more characterization is required for the limitations of this technique to be well understood [15].

As the coating technology begins to solve some of the barriers that previously limited its performance, imaging technology will needed to expand its capabilities in order to continue the progress.

7.2 Pattern Definition

In CD control, the uniformity of the aerial image across the device is the primary factor effecting the quality of the final pattern definition. Even if a uniformly conformal resist coating could be achieved, the focal position and illumination intensity of the aerial image must still conform to the underlying surface to produce a quality photoresist pattern.

Sidewall Profile

The second most important parameter is that of quality sidewall profiles. In general, plating and deep etching place different constraints on the required resist layer characteristics, but both see advantages of nearly vertical sidewalls for the final resist pattern (see Figure 13) [17].

The aerial image of the mask pattern in conventional imaging tools is typically located in a single focal plane. As this image is delivered to a substrate with significant topography, this advantage

works against creating a quality latent image in the resist layer. Whereas techniques such as focus drilling can be used to address the problem in planar thick resist layers, varying topography often will require a different approach.

Other aspects of topography can complicate the transfer of a quality image. For instance, reflections from the substrate in the form of interference patterns can create unwanted variations in the aerial image intensity. These standing wave patterns create a rippled sidewall profile in planar resist layers. On structures with significant topography, the illumination of the angled substrate layer can reflect the exposure energy into unwanted areas as well (see Figure 14). Antireflective coating on the substrate material can be used to reduce this effect by canceling the light that reaches the substrate surface.

Multilayer Masks

One technique of merit is to vary the planarity of the mask image. The basic philosophy is to project an aerial image with a three dimensional focal plane that matches the topographic variations in the substrate surface. It involves either etching the mask surface or building up layers to create a three dimensional surface in the initial pattern image [18, 19]. This opens up the initial constraints on the aerial image to allow wider flexibility in focal plane resolution at the substrate surface.

Another advantage of this approach is that part of the problem of imaging at different levels is shifted from one tool set (conventional UV lithography) to another tool set (e-beam lithography), which has very different constraints on focal imaging.

Multisurface Imaging

One approach to creating images on significantly different levels of topography is to partition the focal plane range into multiple levels. By imaging only those device structures that lie in one focal range level, the image quality can be maintained within acceptable values. Optimally, the device design would cluster critical components at specific topographical levels. This would allow a single field to image all components at that level. Other reticle fields would than be used to image components on other focal levels. As with all techniques, the application requirement for critical structures at multiple levels needs to be justified by the increased performance or unique capability achievable through such a device design.

7.3 Structural Definition

Pattern Transfer/Etch Proximity Effects

Structural definition by deep reactive ion etching has several constraints accentuated by high topography, one of which is the conformality of the plasma sheath. The plasma boundary layer plays a significant role in directing the ions used to bombard the surface during etching. If the variation in topography extends over a sufficient distance, the plasma sheath can sag down into the recesses. This can then change the angle of the accelerated ions, allowing more sidewall erosion

than experienced in other parts of the structure. This aspect ratio dependent etch (ARDE) effect can become a major limitation in the final structure and must be addressed at the initial device design phase.

8.0 Conclusions

The available product space in microelectromechanical structures is bounded by the capabilities of practical pattern transfer processes. The three primary components of pattern transfer processing (predefinition, pattern definition, and structural definition) were discussed, and the importance of their interdependencies was noted. The two key classes of high aspect ratio and high topography structures were reviewed by examining the challenges and some solutions being worked with today. Extending the capabilities in conformal resist coating and enhanced depth of focus techniques are two important areas for expanding MEMS device limitations. Close collaboration between vendors and university work in these areas will be needed.

9.0 Acknowledgments

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Deep silicon etch profiles - Courtesy of Alcatel Comptech

Multilayer mask graphics and SEM - Courtesy of Stanford University [20]

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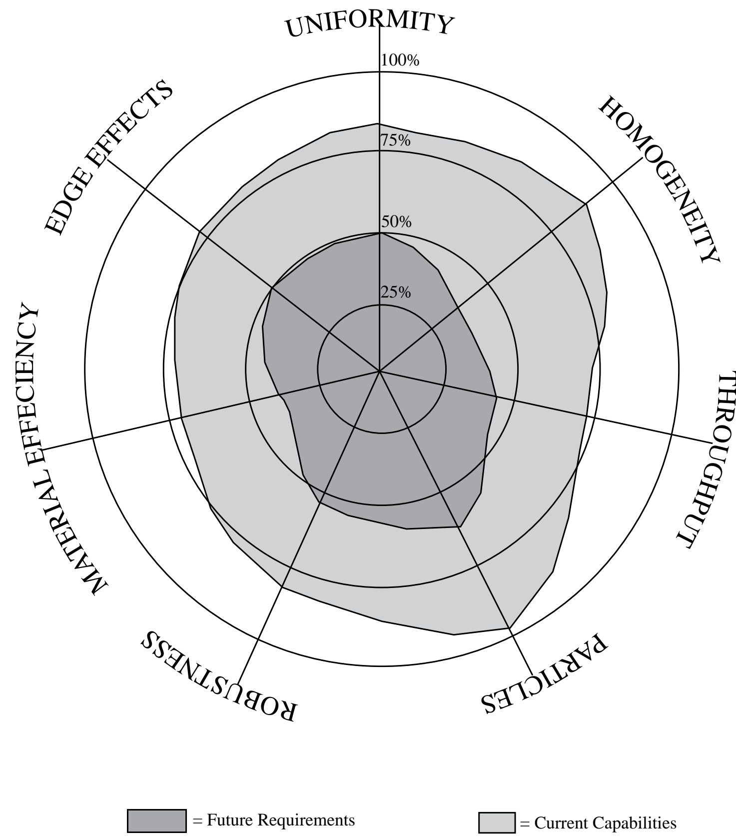

Figure 1: Issues for Coating Technology

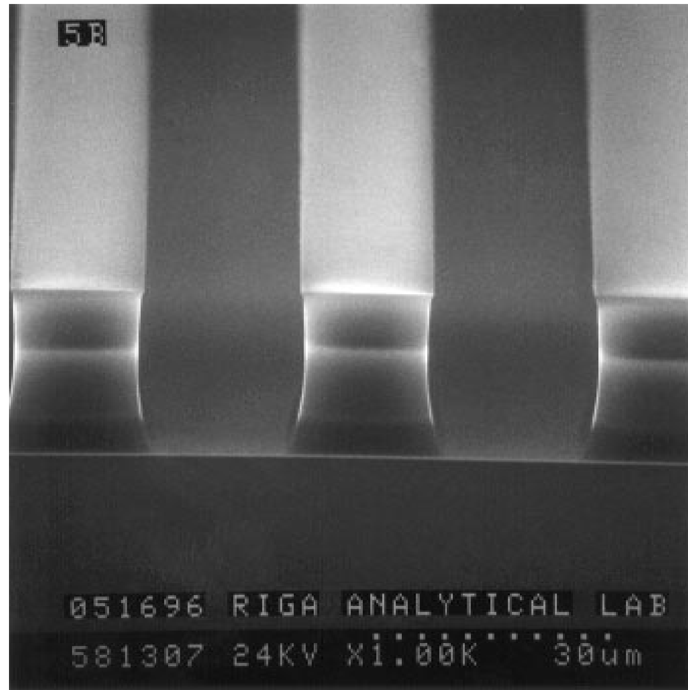

Figure 2: Multilayer Resist Process

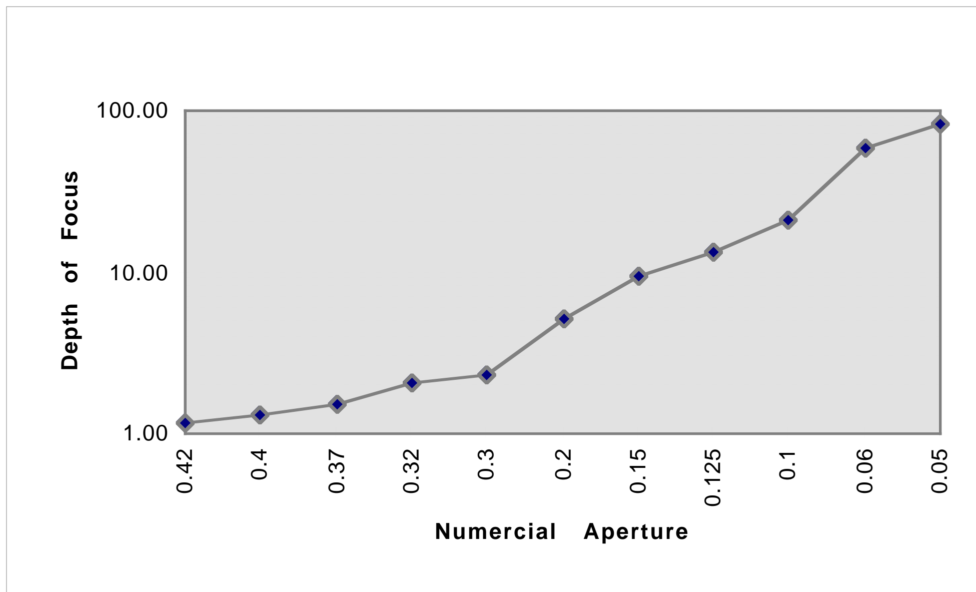

Figure 3: Relationship of Depth of Focus to NA

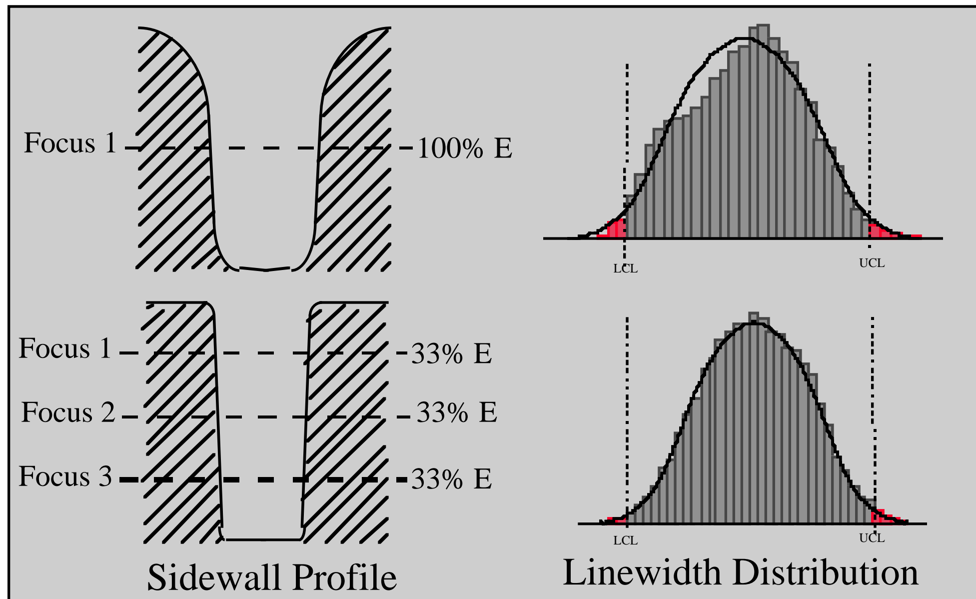

Figure 4: Focus Drilling - Concept and Field Data

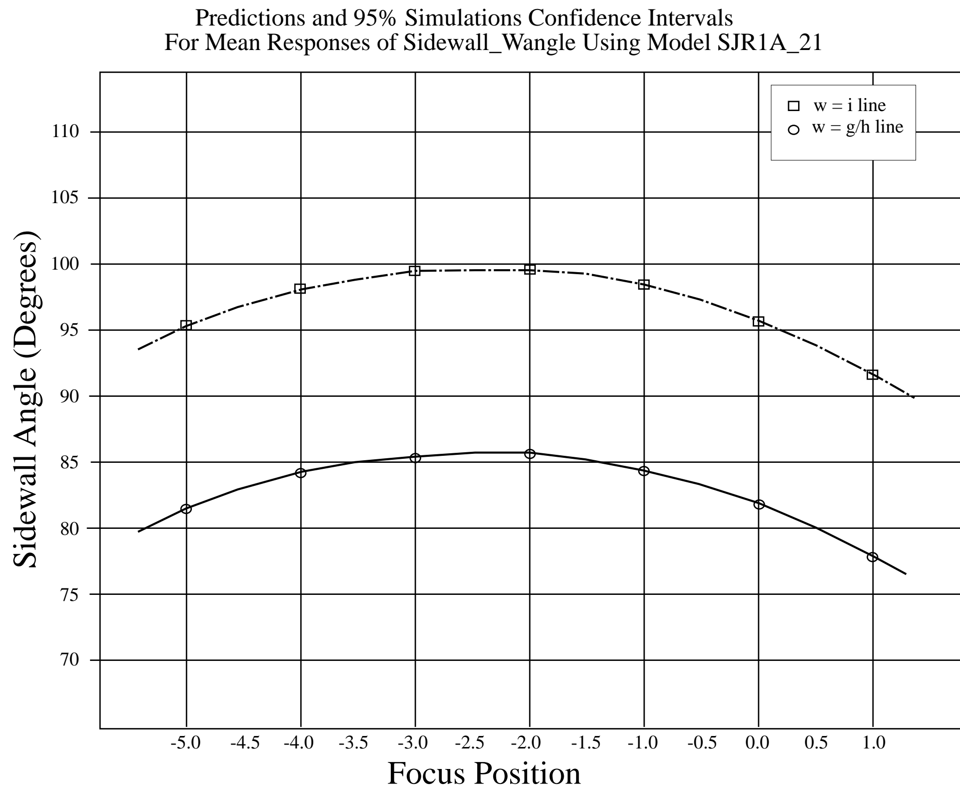

Figure 5: Variation of Sidewall Angle with Focus and Exposure Wavelength

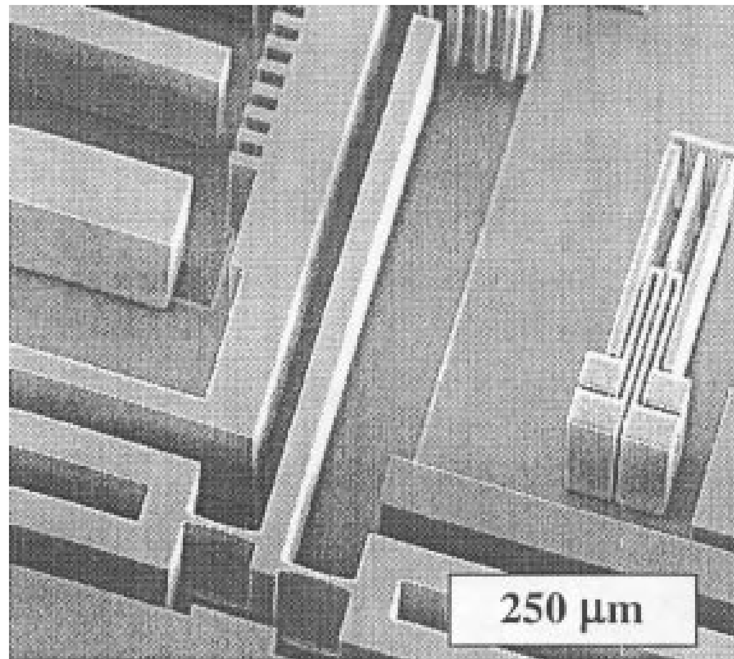

Figure 6: Deep Silicon RIE Etching Profile

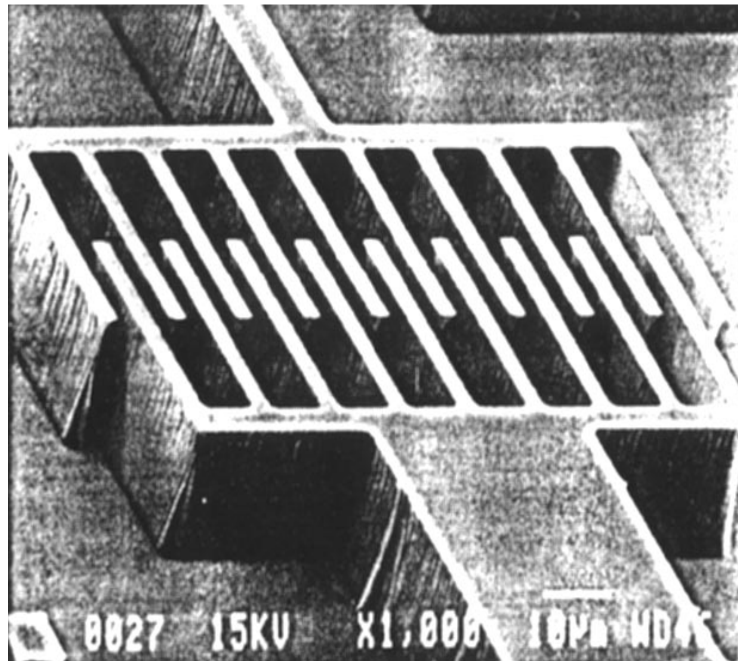

Figure 7: Typical Plating Application

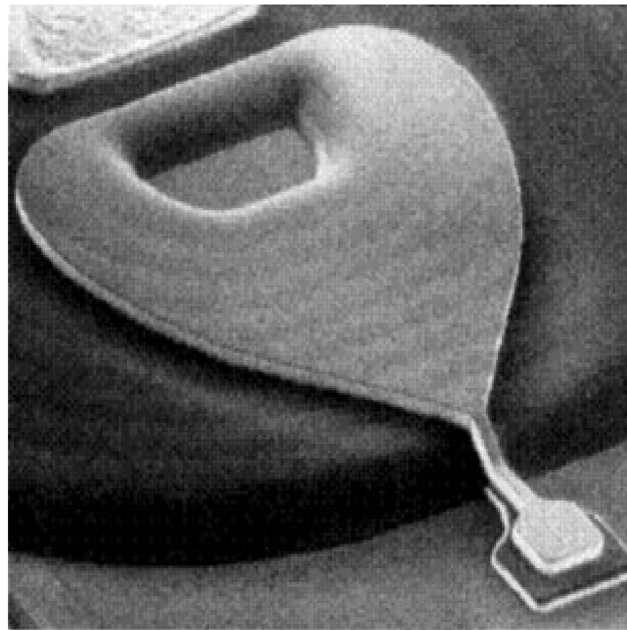

Figure 8: High Topograph Transitional Structure of Thin Film Head

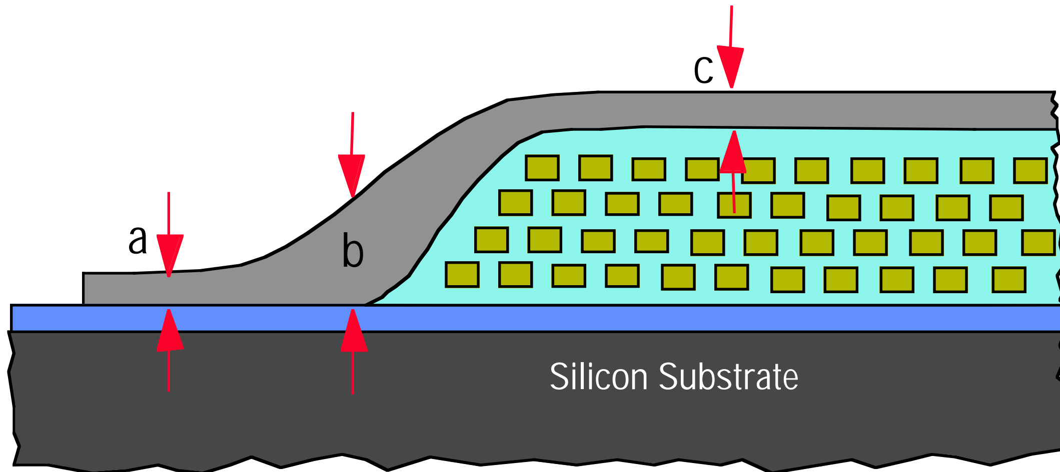

Figure 9: Resist Thinning and Puddling from Topography Change

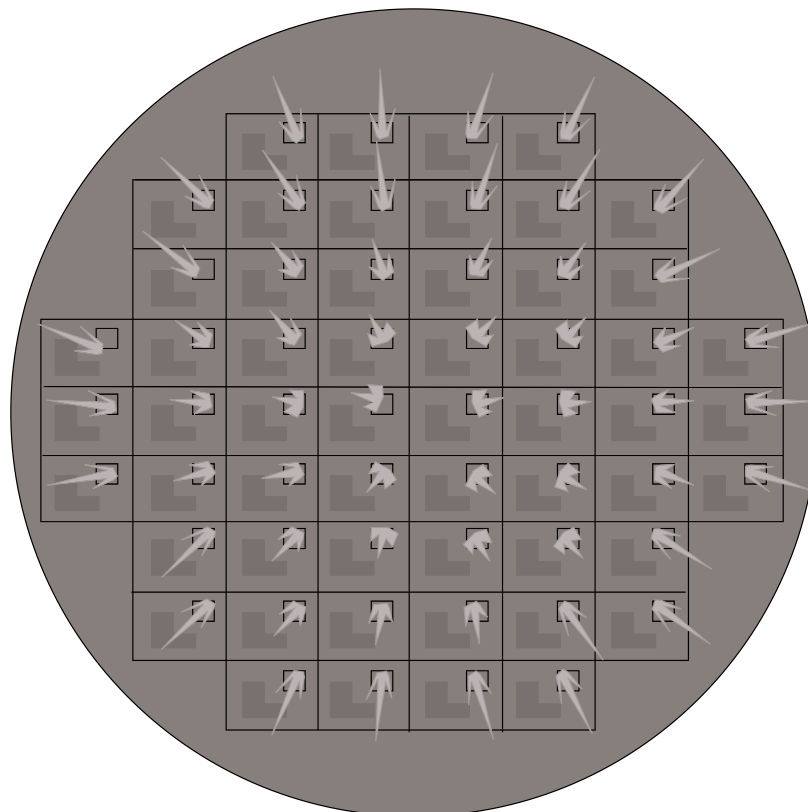

Figure 10: Spin Shadowing from Topography

Figure 11: Multilayer Resist (2 µm lines in 10 µm of resist over 6 µm structures)

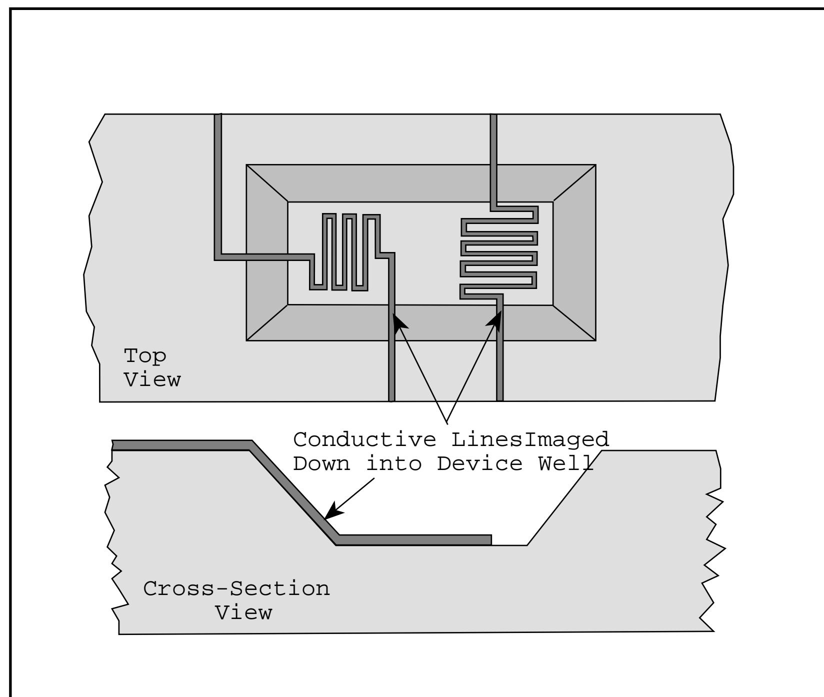

Figure 12: Image Integrity on Oblique Surfaces

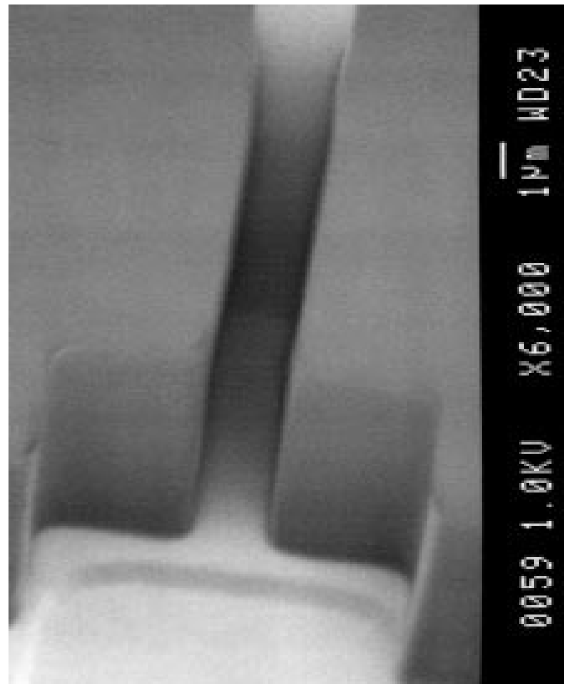

Figure 13: Sidewall Plating Profile in Thick Resist

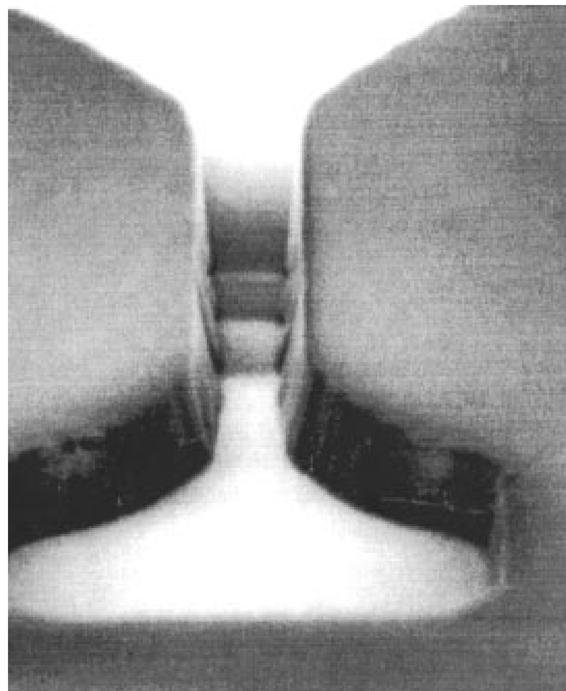

Figure 14: Sidewall Notching from Topography Reflections