

Application of Pattern Recognition in Mix-and-Match Lithography

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Mix-and-match lithography continues to gain acceptance as a valuable strategy for reducing capital costs and increasing throughput productivity in semiconductor manufacturing. The successful implementation of mix-and-match lithography requires consideration of the unique characteristics of all systems being matched. Among these issues are alignment target placement and alignment strategy. The alignment system for each stepper manufacturer uses specially designed targets for wafer alignment. However, the wafer area available for dedicated alignment targets is typically restricted to maximize the quantity of production die per wafer. One approach to remove the target area limitation is to implement an alignment system based on pattern recognition techniques.

Using pattern recognition, the optical image of a specified field structure is digitized and interpreted as an alignment target. Since pattern recognition has the potential to learn and interpret various structures, it provides great flexibility for using alignment structures from other steppers or possibly device structures. This capability minimizes the wafer area required for alignment targets.

Typically, there are two steps involved in wafer alignment in mix-and-match lithography. First is wafer global alignment which is necessary to remove coarse grid placement errors due to wafer loader matching. The second step is the fine or precision alignment of the stepper field prior to exposure. A pattern recognition system provides the capability for either or both of these alignment procedures.

In this study, a pattern recognition system on a Ultratech 2244i stepper is used to demonstrate the elimination of global alignment targets for mix-and-match lithography. The characterization wafers are patterned with a 5x reduction stepper for the first level. Using the first level wafers from this stepper, a performance comparison is made to evaluate the flexibility of the pattern recognition system on a variety of pattern features and substrate films for global alignment. The pattern recognition repeatability and reliability for the case of global alignment is determined. In addition, the MVS capture time and the robustness of the MVS search routines are evaluated as a function of global grid errors.

1.0 INTRODUCTION

Historically, global competition in integrated circuit fabrication has been based on both technological and economic factors. However, fabrication costs are now becoming the single dominant issue as the price of new high-volume production facilities approaches the billion dollar level [1]. Since lithography equipment represents a large fraction of this investment cost, it is a primary area in which to pursue cost savings. One technique that has been extremely successful in containing lithographic costs is mix-and-match lithography [1, 2]. In this approach, a less costly and higher throughput lithography tool is used for noncritical levels, while a higher resolution and more expensive lithography tool is used only on critical levels. A major technical challenge for mix-and-match lithography is the production of advanced technology devices with tight overlay requirements [3].

Successful implementation of mix-and-match lithography between different stepper designs requires consideration of the unique characteristics of each system. This includes optimal field size utilization, field orientation on the wafer, global alignment matching between steppers, optical image orientation, and wafer global and local alignment targets for each stepper design [4]. Lithography tool flexibility in these areas is crucial in meeting the goal of mix-and-match using different steppers from a variety of manufacturers.

One area where stepper designs historically had limited flexibility is alignment systems. Each stepper manufacturer has one or more alignment systems which frequently include bright field detection, dark field detection, two-wavelength detection and bright field TV modes [5,6]. In some cases, alignment systems have been developed to address overlay problems encountered on specific film stacks in a production environment [7]. All alignment systems use specially designed structures that are placed in the lithography field on the wafer. Typically, these target structures are only applicable for a specific alignment system from a given stepper manufacturer. This increases the number of targets which must be placed in a field for mix-and-match lithography.

There are two steps involved in wafer alignment. First is global alignment where the wafer is located in X, Y and theta relative to the wafer stage of the stepper. Global alignment is of particular importance in a mix-and-match environment since alignment target capture depends on how accurately the wafer is placed on the stage. It is common for wafer centering to be consistently offset between stepper types. In practice, each stepper manufacturer has a different technique for global alignment. A special global alignment structure may be required to be placed on the wafer for this step.

The second alignment step is the fine or precision alignment of the stepper fields to support layer to layer registration. Typically, target structures are placed multiple times in a lithography field on several process film stacks to obtain better signal quality for alignment. The result is numerous target types may need to be placed in the field to support the complete fabrication process utilizing several types of steppers. These fine alignment targets are required to fit within the device scribe lanes which limits their number and size. The wafer area available for scribe lanes is

typically restricted to maximize the quantity of production die per wafer. The scribe lanes used at some fabrication facilities are approaching 80 microns and will continue to decrease in size in the future. Thus, finding sufficient wafer area for both global alignment and fine alignment targets can be difficult for mix-and-match lithography.

One approach to remove the limitation on the number of available targets is to implement an alignment system based on pattern recognition techniques. Using this technique, the optical image of a specified structure in the lithography field is digitally stored and interpreted as an alignment target. Since pattern recognition has the potential to learn and interpret various unique structures, it provides great flexibility for using alignment structures from different lithography systems or possibly active area device structures. A pattern recognition system provides the capability for both global and fine alignment procedures. This capability dramatically assists in minimizing the wafer area required for alignment targets.

2.0 Machine Vision System

Pattern recognition has a history of wide use in microelectronic fabrication and testing. Automated inspection technologies use digitized images from die to compare device structures for pattern errors [8]. Both metrology and wire-bonding systems typically use pattern recognition to locate the appropriate structure in a die. Pattern recognition can also be used as part of actual metrology measurement processes [9,10].

An effective pattern recognition system must meet certain basic requirements for mix-and-match lithography. The first is to provide the alignment accuracy and precision necessary to achieve the total overlay budget required for advanced process designs [11]. The second requirement is that the alignment system must not impact the stepper throughput. A high wafer throughput is mandatory to meet the cost-of-ownership requirements for mix-and-match lithography systems. The third requirement is support of user definable alignment targets for maximum flexibility. As discussed in the previous section, user definable targets minimize the number and size of structures required for mix-and-match alignment. The fourth requirement is demonstrated process stability in a production environment. Ultratech Stepper designed a pattern recognition system designated the Machine Vision System (MVS) to meet all of these requirements. MVS has been used in production manufacturing of row-bars using the Ultratech 1700 thin film head system [12]. In addition, MVS is a standard feature of the Ultratech 2244i Stepper, which was specifically designed for mix-and-match applications.

Figure 1 shows the general setup of the MVS. The machine vision system is a through-the-lens (TTL) tool which aligns the wafer with the reticle pattern by using position measurements from both images. The target image on the wafer is projected and referenced to a key image on a reticle which can be viewed on a VGA monitor. The image is then sent to a charged coupled detector (CCD) camera and a Cognex[®] 4200 image processing unit. The Cognex[®] is a commercially

available system used to capture, identify and determine an image distance from a reference location. The distance information generated by the MVS is used by the steppers control system to provide positioning information for alignment of the wafer. In actual practice two camera systems are used for the right and left side of the lithography field to remove any rotation error between the wafer and reticle.

The MVS imaging lens use the 520 to 590 nm spectral band for wafer alignment while filtering out the exposure wavelengths. The system has a numerical aperture of 0.25 and partial coherence of 0.8 which provides the optimum combination of viewing size and depth of focus. The lens system is a telecentric design for maximum performance and elimination of shadowing. The MVS system used on the Ultratech 1700 for thin-film heads has a 20x magnification which provides 2 pixels per micron. MVS systems for mix-and-match lithography will provide enhanced alignment capabilities by utilizing more pixels per micron.

A tungsten-halogen lamp provides illumination of the MVS keys and targets as shown in figure 2. The illuminator lamp output is focused on a fiber optic bundle which passes light through a series of lenses for collimation. The light then passes to a beam splitter and is focused through a flipping prism on the chrome side of the reticle. The flipping prism is used because of space limitations between the stepper lens and illuminator to direct light towards the back of the stepper where the TTL lens and CCD cameras are located. The MVS utilizes a 300 by 300 micron viewing window on the reticle. Any keys in the reticle viewing window reflect energy and are imaged back through the lens. The energy which strikes the wafer illuminates the target and is reflected back through the main lens, through the reticle window and imaging lens through the beam splitter. A multi-mirror folded camera box directs the combined images back to a CCD video camera. A video image from this camera is provided to the Cognex[®] system for signal processing.

The MVS package functions as a second alignment system on the Ultratech Stepper. It can be used in conjunction with the dark field alignment system (WAS) which is standard on all Ultratech Steppers [13]. This provides flexibility in using either the MVS or WAS for the wafer global alignment and fine alignment operations. For the initial studies in this paper the MVS system is used for wafer global alignment and the WAS is used for fine alignment.

3.0 EXPERIMENTAL METHODS

3.1 Lithography and Processing

The MVS sample wafers for this study were prepared by patterning the first level using a Canon 2500i2 stepper with a field size of 22 x 22 mm square. These wafers were processed into three groups and processed to simulate major parts of a submicron CMOS manufacturing process. These groups included a poly level film stack, tungsten plug film stack, and contact level stack as illustrated in figures 3a, 3b and 3c. The wafers were then coated with 1.0 microns of JSR IX

500EL photoresist for second level patterning on an Ultratech 2244i. The Ultratech 2244i was matched to the Canon 2500i2 with two 5x reduction fields aligned to a single 22 x 44 mm field. The Ultratech MVS was used for wafer global alignment and the WAS was used for fine alignment.

Global alignment of the wafer using the MVS system involves two steps. The first is a search sequence for the previously selected global alignment target using the left MVS camera. The search consists of a square spiral search using a 0.1 mm stage step size as shown in figure 4. After the global alignment target is captured with the left camera, the stepper then performs an arc search of the wafer using the right MVS camera to remove any rotation error. Following the MVS global alignment, the stepper then transfers to the WAS for fine alignment of the wafer. The required placement accuracy from the MVS global alignment is set by the WAS scan distance, which is 1/4 of the size of the fine alignment target. Thus for an 80 micron target the required MVS accuracy for global alignment would be 20 microns. The occurrence of any failures and residual positional errors for the WAS were used as response criteria to gauge MVS performance for global alignment.

3.2 MVS Alignment Targets

Five unique field structures patterned on the first level wafers were selected for the MVS pattern recognition testing. Figure 5 depicts each target pattern as seen through the MVS viewing window of 300 by 300 microns in size. The first MVS target is a “X” shape which was selected for its diagonal structure and wide linewidth. These characteristics suggest it will be insensitive to process variations and is a unique pattern which reduces false target captures. The second MVS target is cross contained within a single box, which is representative of the fine alignment targets used by the WAS on the Ultratech 2244i. The third MVS target is a cross within a double box. This is an alignment structure used by the 5x reduction stepper. The additional box structure and wider cross dimensions on this target make an interesting comparison to target 2. The fourth MVS target used the first seven characters of the word “SEMATECH”. Note this appears a mirror image on the wafer due to the image transfer relative to the reduction reticle. This structure shows the flexibility of the MVS in terms of capturing any unique structure in the lithography field. The fifth MVS target consisted of short horizontal segments enclosed by a rectangle which is part of a metrology structure. Note that the white elbow bracket in the lower left corner of each image is the reticle key structure as described in figure 1.

3.3 Experimental Design

A series of experiments were performed to evaluate the reliability and process latitude of the MVS. The design factors examined in this study were the five MVS target patterns and the three different groups of processed wafers. The first experiment involved validation of the MVS capture of all target types for each type of process wafer. This was measured by successful MVS capture and subsequent fine alignment using the WAS on the 2244i.

Additional experiments were performed to evaluate global alignment repeatability and system reliability. Global alignment repeatability was measured in two separate modes. Dynamic repeatability was demonstrated for multiple reforest evaluate wafer-to-wafer effects such as grid errors and processing variations. Static repeatability was demonstrated using the same wafer in a continuous cycle to monitor stepper and MVS errors. Reliability of the MVS system was evaluated by monitoring for prealignment failures in wafer cycling over a period of days.

Three separate experiments were performed to characterize MVS capture time and search routines as a function of global wafer grid errors. First, MVS capture time as a function of X and Y wafer loading errors was measured. This test was intended to demonstrate the effects of systematic or random grid errors on MVS performance. For the second test, MVS capture time versus directional offset was evaluated to characterize the effectiveness of the MVS search routine. The third experiment examined the impact of global wafer rotation on capture time. These three experiments were performed using MVS target 1 and wafers with the poly level film stack.

4.0 RESULTS AND DISCUSSIONS

4.1 MVS Target Capture

The MVS capture of each of the five target patterns was verified using wafers from all three types of process wafers. There were no MVS capture failures for any of these 15 test cases. In addition, wafers were successfully aligned using the MVS for global alignment and the WAS for fine alignment for all five MVS targets and three types of process wafers. This shows the robustness of the MVS system and its flexibility in using any unique structure as a global alignment target.

4.2 Global Alignment Repeatability and Reliability

Global alignment repeatability was measured using both dynamic and static tests. Dynamic repeatability was demonstrated for each MVS target by aligning a minimum of 5 wafers from the same process group in sequence. This was repeated five times for a total of 25 separate wafer-to-wafer tests. There were no alignment failures in any case. Static repeatability was demonstrated by aligning the same wafer sequentially as many as 960 times. Again, there were no alignment failures for any MVS target. Reliability of the MVS system was evaluated by long term wafer cycling over a period of days. The same wafer was aligned a minimum of 120 times each day for three consecutive days. Again, there no MVS alignment failures were observed. These repeatability and reliability tests clearly demonstrate the effectiveness of the MVS for global alignment in mix-and-match lithography.

4.3 MVS Capture Time

4.3.1 X and Y Loading Error

Three separate experiments were performed to characterize MVS capture time and reliability as a function of global wafer grid error. In the first experiment MVS capture time as a function of wafer loading error was measured by intentionally introducing grid offsets of up to 1.0 mm on the Ultratech 2244i. The time required to capture the global alignment target was then measured. The MVS capture time as a function of offset error is shown in figure 6. Graphs for both X and Y offsets show extremely rapid capture for loading errors less than 0.2 mm. Since wafer centering can usually be matched between steppers to less than 0.1 mm, these results suggest that the MVS should be able to routinely capture global targets in less than 5 seconds [4].

The MVS capture time shows a strong nonlinear dependence because of the spiral search routine. Since the spiral search time is a function of the search area, it is reasonable to expect the search time to depend on the square of the linear offset. To test this hypothesis, a second order regression analysis was performed. Quadratic curve fits for both X and Y offsets are shown in figure 6. In both cases, the goodness of fit was in excess of 0.99. This strong correlation supports that the spiral search is proportional to the square of the offset distance.

4.3.2 Directional Offset Errors

For the second experiment, MVS capture time versus directional offset was evaluated to characterize the effectiveness of the search routine. Grid offsets of 0.35 and 0.5 mm were intentionally introduced at angles varying from 0 to 360 degrees. The time required to capture the global alignment target was then measured. The MVS capture time as a function of angle is shown in polar coordinates in figure 7. It is immediately apparent that the capture time is longer at 90°, 180° and 270° angles. Careful examination of the square spiral search routine shown in figure 4 suggests an explanation. Offsets near angles of 45°, 135°, 225° and 315° should be more quickly captured because the center of the search field at these locations is the $\sqrt{2}$ farther from the origin than corresponding search locations 0°, 90°, 180° and 270°. The rapid capture at 0° can be explained in terms of the starting direction of the square spiral search. It starts in the +X direction which reduces the time to capture in this direction. This can be more easily visualized by looking at an idealized contour plot of the total number of search steps as a function of X and Y step offsets as shown in figure 8. It is apparent that there is target capture with fewer steps in the +X and +Y directions.

4.3.3 Global Wafer Rotation Errors

The third experiment examined the impact of global wafer rotation on capture time. Rotation errors were intentionally introduced and the time for the left camera to capture the global target was measured. After the global alignment target is captured with the left camera, the stepper then performs an arc search of the wafer using the right MVS camera to remove any rotation error. The

time for the right camera to capture the target was measured. These two times were added together to determine the total global target capture time. The capture time as a function of rotation error is shown in figure 9. It is apparent that rotation errors less than 5 milliradians can be captured in under five seconds. Rotation errors larger than 5 milliradians would not be expected in a controlled production environment.

5.0 CONCLUSIONS

Since pattern recognition has the potential to learn and interpret various unique structures, it provides great flexibility for using alignment structures from different lithography systems or active area device structures. A pattern recognition system provides the capability for both global and fine alignment procedures. This capability dramatically assists in minimizing the wafer area required for alignment targets.

The machine vision system on a Ultratech 2244i stepper has been used to demonstrate the elimination of global alignment targets for mix-and-match lithography with a 5x reduction stepper. Wafers were successfully aligned using the MVS for global alignment and the darkfield WAS for fine alignment for five different MVS target structures and three types of submicron CMOS process wafers. These results demonstrated the robustness of the MVS system and its flexibility in using any unique structure as a global alignment target.

The pattern recognition repeatability and reliability for global alignment was established using both dynamic and static testing techniques. No MVS alignment failures were observed in sequential test runs of up to 960 wafers. In addition, three separate experiments were performed to characterize MVS capture time and the robustness of the MVS search routines. These results suggest that the MVS should be able to routinely capture global targets in less than 5 seconds for the typical wafer centering and rotation errors that would be encountered in a controlled production environment.

Future work will extend the MVS for use in pattern recognition for fine alignment. Using MVS for combined global alignment and fine alignment will offer enhanced capabilities for mix-and-match lithography.

6.0 ACKNOWLEDGMENTS

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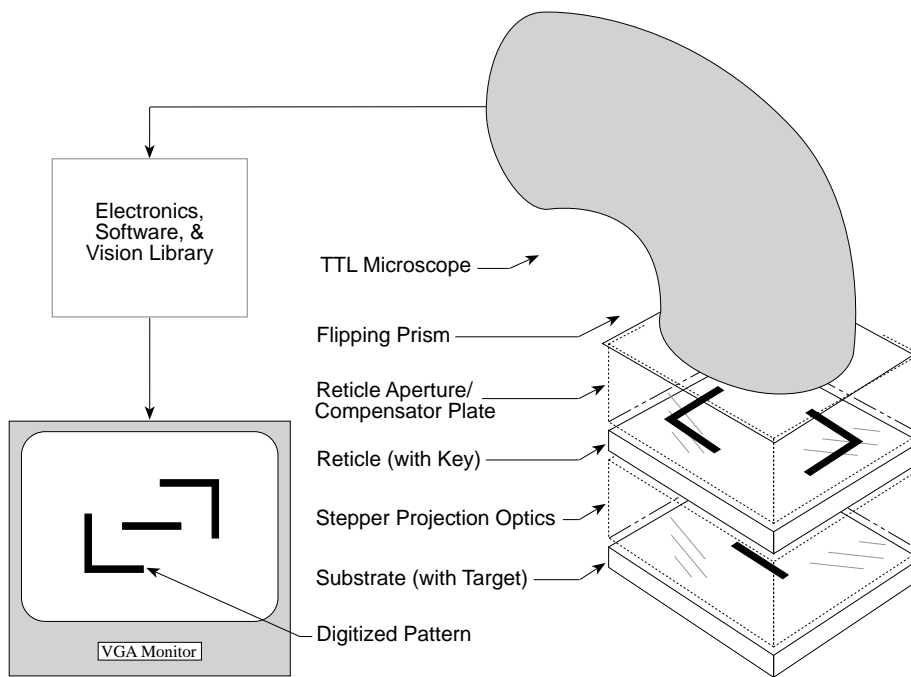


Figure 1: General MVS System

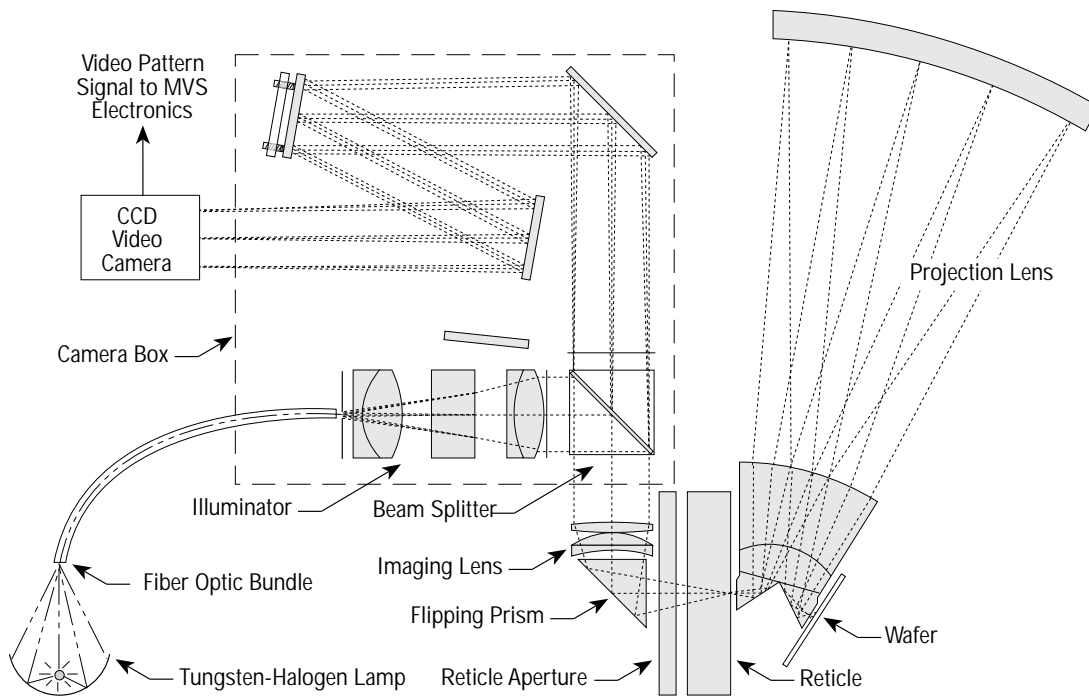
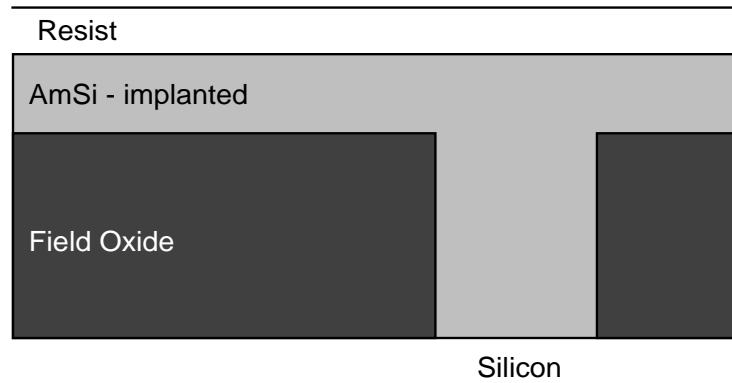
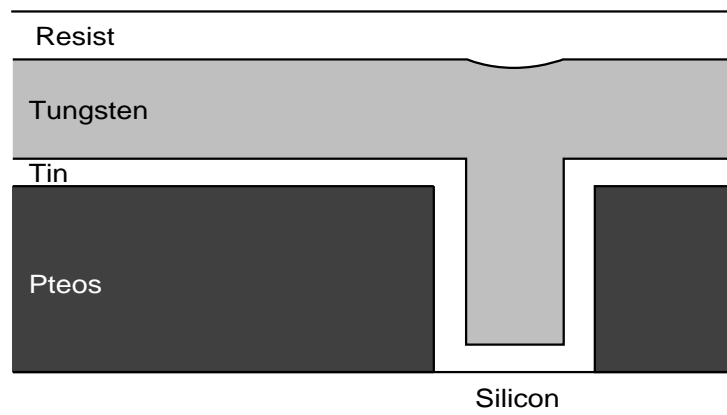


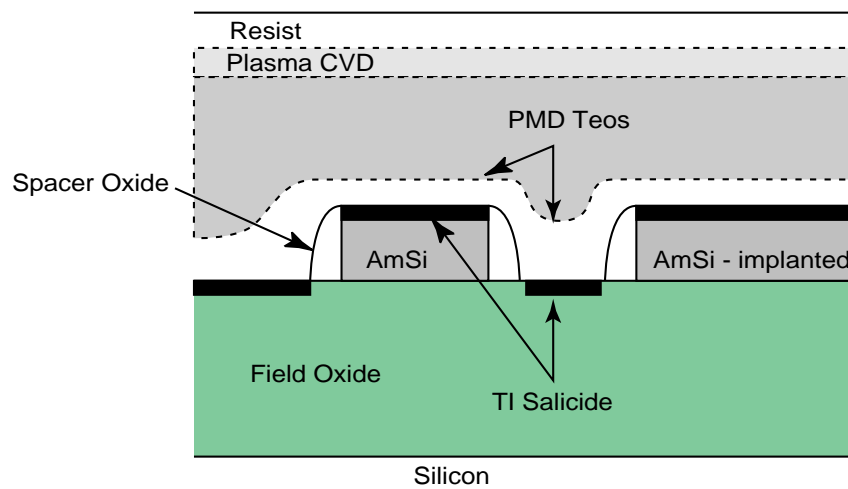
Figure 2: MVS Optical Components



(A) Poly level film stack



(B) Tungsten plug film stack



(C) Contact film stack

Figure 3: CMOS processes evaluated for MVS alignment testing.

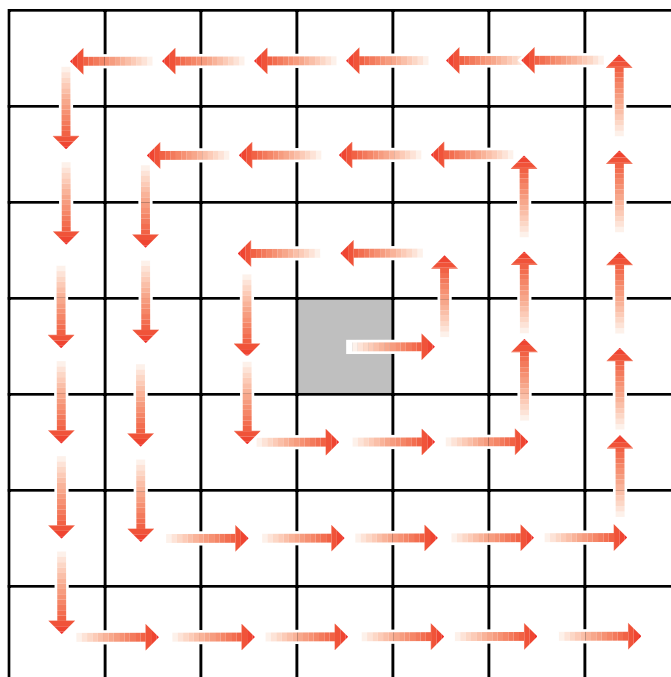


Figure 4: Square spiral search routine used by the MVS.

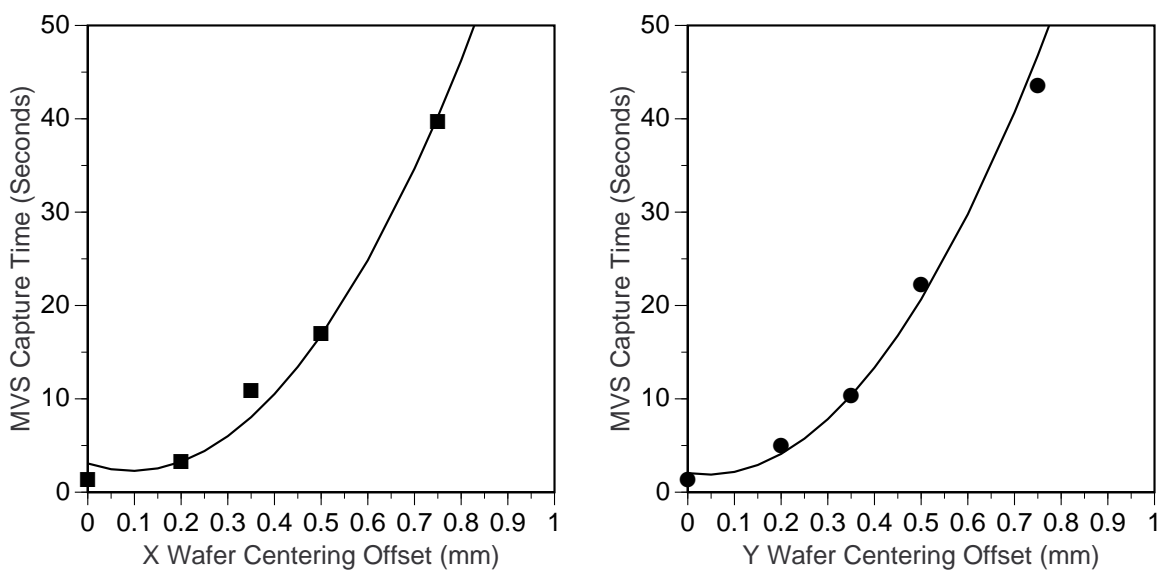
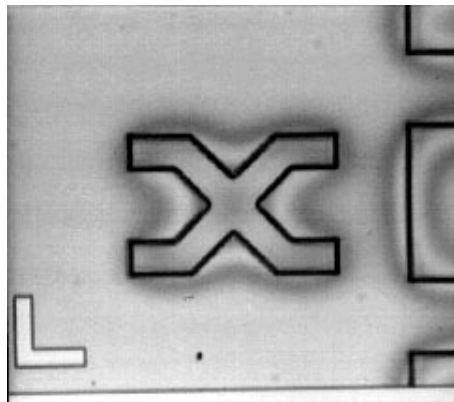
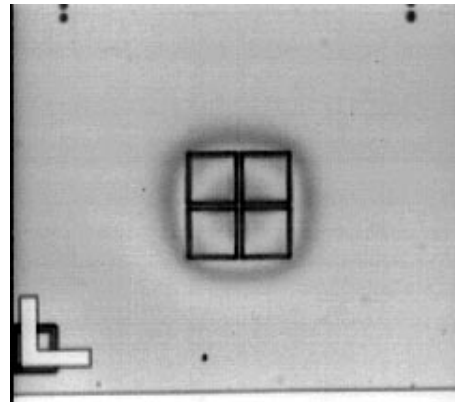


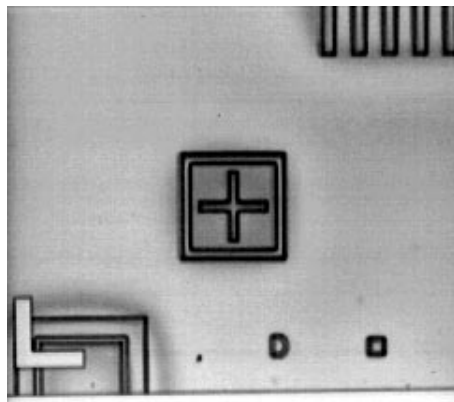
Figure 6: MVS capture time (seconds) as a function of X and Y centering offsets (mm).



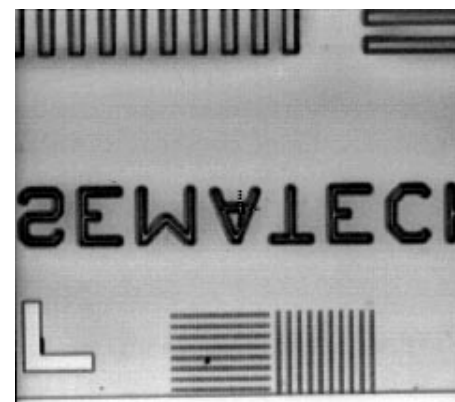
MVS Target 1



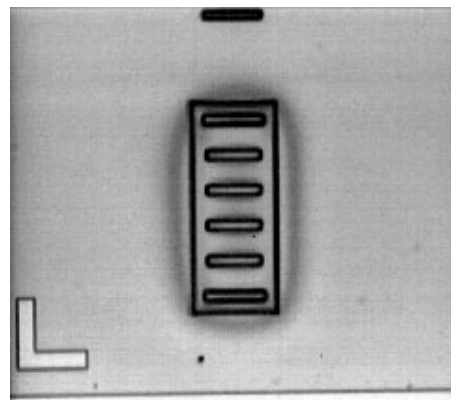
MVS Target 2



MVS Target 3



MVS Target 4



MVS Target 5

Figure 5: Five alignment structures evaluated for MVS pattern recognition testing.

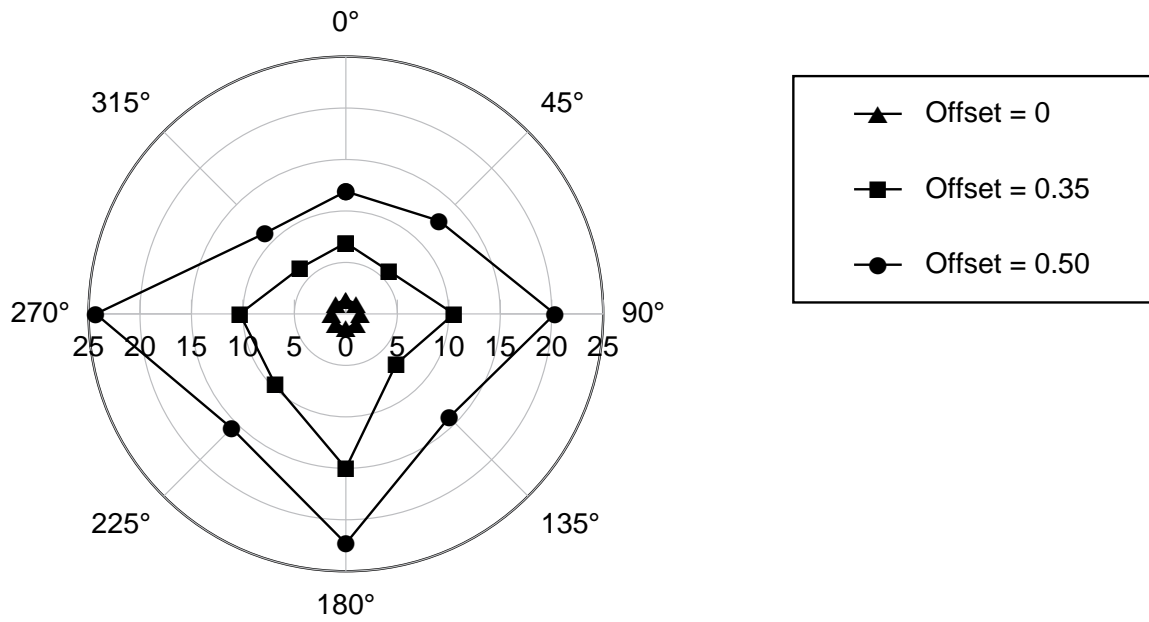


Figure 7: MVS capture time (seconds) as a function of angle (degrees) and offset magnitude (mm).

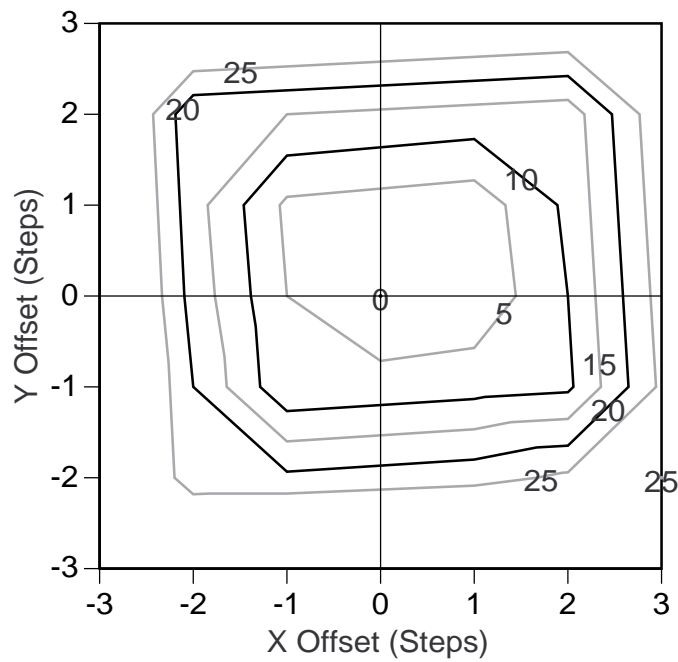


Figure 8: Idealized contour plot of the total number of search steps as a function of X and Y offsets units of step size.

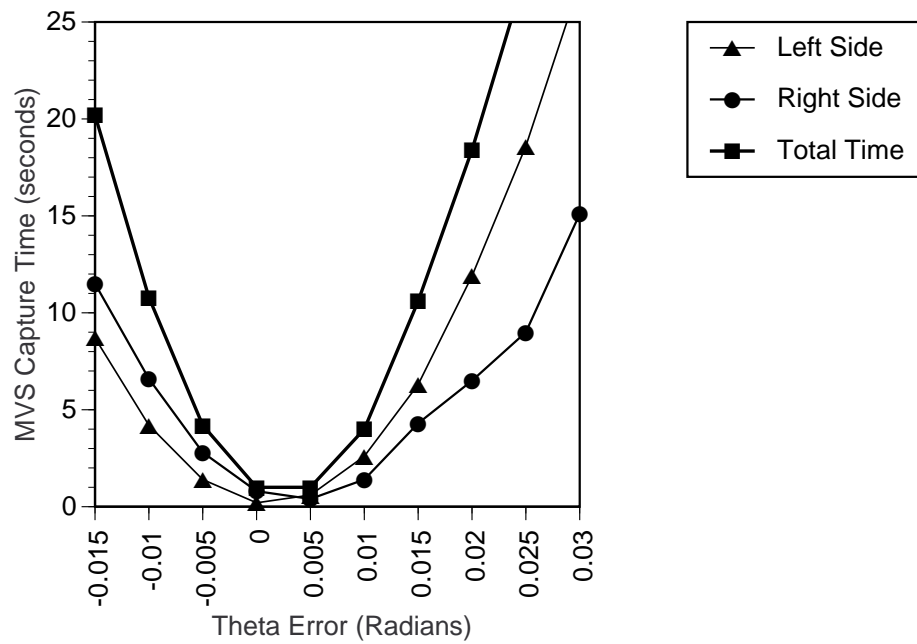


Figure 9: MVS capture time (seconds) as a function of wafer rotation error in radians.